THESIS

HIGH EFFICIENCY THERMOELECTRIC DEVICES FABRICATED USING QUANTUM WELL CONFINEMENT TECHNIQUES

Submitted by

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ABSTRACT

HIGH EFFICIENCY THERMOELECTRIC DEVICES FABRICATED

USING QUANTUM WELL CONFINEMENT TECHNIQUES

Experimental results are presented of thermoelectric materials, specifically two-dimensional quantum well confinement structures, formed by ion beam sputter deposition methods. Applications of these thermoelectric devices include nearly any system that generates heat including waste heat. The targeted applications of this research include harvesting of waste heat from stand-alone generator systems and automobiles. Thermoelectric generator modules based on an in-plane orientation of nano-scale, thin-film, superlattices have demonstrated very high performance and are appropriate for a wide range of waste heat recovery applications. In this project, a fast, ion-beam-based deposition process was developed for producing Si/SiC (n-type) and B_4C/B_9C (p-type) superlattices. The deposition process uses low-cost powder targets, a simplified substrate holder with embedded heater, a QCM deposition rate monitor, and stepper-motor-controlled masks. Deposition times for individual layers are shown to be significantly shorter than those achieved in magnetron-based systems. As an example of the speed of the process, a 10-nm thick Si layer can be deposited in as little as 20 sec while a SiC layer can be deposited in less than 100 sec. Electrical resistivities, thermal conductivities and Seebeck coefficients are reported for the deposited films as well as their respective non-dimensional figures of merit (zT). Figures of merit (zT) approaching 20 at modest temperatures of ~600 K were observed. These measurements are made in-plane where enhanced Seebeck values and reduced electrical resistivities have also been reported in the literature. A method for directly measuring thermal conductivity in the

plane of the superlattice is described that uses MEMs-based SiN cantilevers. Results are presented for various deposition variables, including film thickness, temperature, deposition energy, and material. Scanning white light interferometry (SWLI) and scanning electron microscopy (SEM) were used to characterize film thickness. In addition to the experimental effort, an analysis was performed to predict the performance of a thermoelectric module fabricated with the superlattice films deposited on ceramic substrates. Thermal efficiencies approaching 15% are predicted for modest cold and hot side temperatures. Thermal conduction through the substrate was found to be the largest factor limiting the performance of the modeled thermoelectric module.

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INTRODUCTION

Solid state thermoelectric devices have the potential to utilize waste heat both in industrial and automotive applications. One of the major challenges is to develop material systems that have high thermoelectric figures of merit, zT, in the temperature ranges of interest. In recent years, nanoscale fabrication techniques have produced several promising new materials with zT greater than 1. An excellent review of traditional materials, like Bi_2Te_3 and PbTe with peak zT near 1, and newer materials that utilize nanostructured features is given by Snyder (2008). Note: z is a material property, with units of K^{-1} for instance, that varies as a function of temperature. When multiplied by the average operating temperature, T, the non-dimensional figure of merit zT is obtained. One class of material that shows promise is thin-film superlattices, where each n-type and p-type film is composed of hundreds of thin alternating layers of two materials. In this work, we investigate n-type films composed of alternating silicon (Si) and silicon-carbide (SiC), and p-type films composed of alternating layers of two types of boron-carbide, B_4C and B_9C. These films have shown excellent thermoelectric properties in the 250-500 °C temperature range, appropriate for waste heat recovery from hot combustion gases that are exhausted from internal combustion engines. For instance, a zT near 4 at 250 °C has been indicated for a $Si/Si_{0.8}Ge_{0.2}$ - B_4C/B_9C couple (2003 Ghamaty), and an average zT of 3 has been observed for a $Si/Si_{0.8}Ge_{0.2}$ - B_4C/B_9C couple operating over a roughly 70 to 250 °C temperature range (Elsner 2009). The high figure of merit of superlattice films is due to quantum well effects, increasing the density of states and the Seebeck coefficient, and scattering of phonons at layer boundaries (Snyder and Toberer 2008). Improvements in the figure of merit for superlattice films are also due to enhanced electrical conductivity.

Estimates vary depending on the degree of system integration and on driving conditions, but the U.S. Department of Energy target of 10% fuel reduction appears to be within reach if thermoelectric modules could be built using these higher zT materials (Bell L. E., 2002).

Average ZT in the range from 1.5 to 2 would enable substantial waste-heat harvesting and primary power-generation. Note: capital ZT refers to the performance of a complete working module rather than just the material property zT. Various government-sponsored programs are underway in the United States and Japan to increase vehicle mileage by converting a fraction of the waste heat in the exhaust systems of trucks and cars to electric power (Bass, Elsneer, & Leavitt, 1994), (Ikoma, Munekiyo, Furuya, Izumi, & Shinohara, 1998).

If the average ZT reaches 2, room, home, and commercial solid-state heating, ventilating, and air-cooling systems become practical. The refrigeration systems would replace R-134A, which when released into the atmosphere has a green- house gas equivalence of 1430 times that of CO_2 (Forester, 2007).

Net gains of about 5 to 10% in thermal efficiency would be possible in diesel-powered generators that are becoming widely used for onsite power generation in the sub MW level to the many 10 MW level. In a commonly proposed cogenerator concept, the solar spectrum is split into shorter wavelengths that yield high photovoltaic-conversion efficiency and longer wavelengths that heat a TE generator (Tritt, Bottner, & Chen, 2008).

At a ZT of 2 and above, cooling and temperature control of microprocessors, communications circuitry, electro-optical systems, and other electronic components become attractive using thermoelectric coolers. The clock speed and operating life of many chip circuits decreases rapidly with increased temperature, so that effective thermal management becomes beneficial on several counts (Jain & Ramanathan, 2006).

An average of 383 million gallons of gasoline is used per day in the U.S. This corresponds to daily consumer spending of nearly $1.4 billion not counting the environmental cost of this consumption rate (U.S. Energy Administration Corporation, 2011). Assuming the use of a thermoelectric module described herein and the efficiency presented, daily savings of 28 million gallons of gasoline could be achieved or $100 million per day in consumer spending. A reduction in gasoline consumption of this magnitude would remove 70 million kg of CO_2 from being emitted into the atmosphere per day (Office of Transportation, 2005). Thermoelectric devices fabricated using quantum well techniques when compared to current leading bulk TE materials are predicted to be 3 times as efficient.

Potential thermoelectric applications range from radioisotope-based satellite power systems to automotive waste heat recovery. Many other applications exist, for example, recently a need to charge cell phones in third world countries has become essential. From 2001 to 2007 mobile phone coverage has increased to over 78 percent. This has led to a 20 percent decrease in the variation in grain prices across the country due to improved communication between consumers and buyers. (Aker, 2008) Similarly cell phones have allowed health-care workers in the rural southeast of Niger to summon ambulances to distant clinics that was previously impossible, however, a central problem remains; the ability to charge cell phones. (LaFraniere, 2005) Thermoelectrics could be the solution to this problem by using waste heat from a cook stove or fire so individuals could charge their phones in their homes rather than having to walk several miles to charge them at a generator station.

If the final enabling advancement, higher ZT, is realized, then efficient solid-state home, industrial, and automotive air conditioning and heating would become practical. In power generation, fuel consumption and CO_2 emissions would be reduced by electric power production from vehicle waste exhaust. Industrial waste-heat recovery systems could reduce emissions by providing supplemental

electrical power without burning additional fossil fuel. TE solid-state heat engines could well play a crucial role in addressing some of the sustainability issues we face today. (Bell L. E., 2008)

In this work, we investigated the performance of Si/SiC and B_4C/B_9C superlattice films deposited on planar silicon wafer substrates. The depositions were performed using an ion beam sputtering system. The films were tested at Colorado State University (CSU) to determine their Seebeck coefficient and electrical resistivity. Further, a micro-scale silicon nitride-based device was used to examine the thermal conductivity of an n-type film at the University of Denver. Taken together, our measurements give best-value figures of merit, zT, for the Si/SiC and B_4C/B_9C films of 8.4 ± 2.1 at 377 °C and 25.0 ± 6.3 at 377 °C, respectively. These very high values of zT have also been observed by (Leavitt, Krommenhoek, Ghamaty, & Elsner, 2010) who used magnetron based deposition techniques.

The primary disadvantage of using superlattice materials arises in the slow speed of manufacturing, which results in high costs. Our ion-beam technique shows the promise of being faster than the magnetron technique which may help reduce the cost of producing these promising materials. Also, compressive or tensile stresses within the thin films can cause the superlattices to crack and delaminate from the substrate. These stresses can be relieved by annealing in vacuum or by using an ion assist (Windischmann, 1992).

RESEARCH GOAL

The focus of this research is to create and characterize quantum well thermoelectric materials. The primary goal is to define deposition conditions and film dimensions that result in the most desirable thermal conductivity, electrical conductivity and Seebeck coefficient. This research is considered important because currently available bulk thermoelectric materials result in very poor devices. The potential of quantum confinement devices is their increased efficiency, resulting in a significant increase in their use in practical applications like waste heat recovery or Peltier cooling.

NOMENCLATURE

Symbol	Units	Description
A	m^2	Area
e	C	Electron charge, 1.602×10^{-9} *C*
E	J or eV	Energy
F	N	Force
I, J	A	Current
k_B	J/K	Boltzmann constant, 1.38065×10^{-23} J/K
m_e	kg	Electron mass, 9.109×10^{-31} *kg*
m	sccm	Gas flow rate in vacuum
P_t	Torr	Vacuum tank pressure
V_B	V	Beam Voltage
I_B	mA	Beam Current
T_s	°C	Substrate Temperature
zT	---	Non-Dimensional Figure of Merit referring to only the specific generating materials
ZT	---	Non-Dimensional Figure of Merit referring to a complete thermoelectric module
α	mV/K	Seebeck Coefficient
κ	W/m^2K	Thermal Conductivity
σ	mΩ·cm	Electrical Resistivity

BACKGROUND

In this research, thermoelectric materials exhibiting quantum low-dimensional effects were created using an ion beam deposition process. A short background into thermoelectricity and the deposition process is given first to place the achieved research in context.

THERMOELECTRICITY

Thermoelectric materials are utilized for power generation in remote locations, on spacecraft used for interplanetary exploration and in places where waste heat can be recovered. While traditional thermoelectric devices have offered good reliability, durability, and little performance degradation over time, more comprehensive usage has been restricted by very low system efficiency and power-specific cost ($/W) of existing devices (Bell L. E., 2008). For instance, (Vining, 2009) estimates that using the common thermoelectric materials available at present, efficiency is limited to perhaps 1/6th of the maximum possible Carnot efficiency. Materials with a zT > 6 can lead to a factor of 2 to 3 improvement in thermodynamic efficiency. The thermodynamic efficiency of a thermoelectric power generator is

Equation 1 – Thermodynamic efficiency of a thermoelectric power generator

$$\eta = \frac{\Delta T / T_h}{2 + \frac{4}{Z \cdot T_h} - \frac{1}{2}\frac{\Delta T}{T_h}}$$

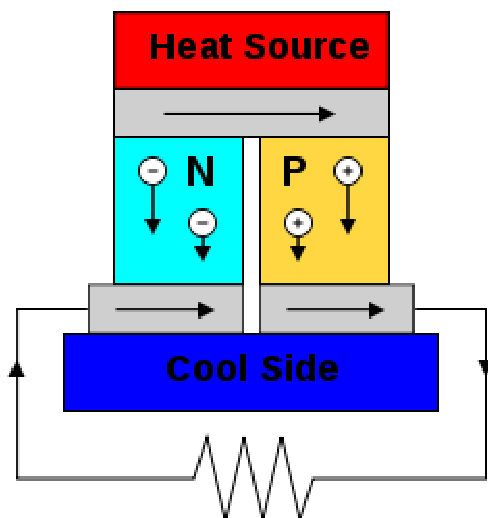
where T_h is the absolute temperature at the hot junction and T_c is the absolute temperature at the cold junction. If the overall figure of merit for the device, Z, is high, the efficiency of the power generator will also be high. For this to be achieved the figures of merit of the thermoelectric materials used to construct the device must also be high. For a specific material, z is defined as:

Equation 2 – thermoelectric specific material z

$$z = \frac{\sigma \alpha^2}{\kappa_{ph} + \kappa_{el}}$$

where σ is the electrical conductivity, α is the Seebeck coefficient, κ_{ph} is the phonon contribution to the thermal conductivity, and κ_{el} is the electronic contribution to the thermal conductivity. Note that κ_{ph} is also known as κ_L, the lattice thermal conductivity. Much of the effort to improve Z over the past 20-30 years has focused on attempts to reduce κ_L without adversely affecting the electrical conductivity. Some success has been achieved with solid-solution alloying. Further reductions in κ_L have been achieved by reducing the grain size of silicon-germanium alloys; however, the potential future benefits of this approach are relatively small. (Elsner & Ghamaty, 1999)

The overall figure of merit for a particular n-p couple operated at a given T_H - T_C range can be found by calculating averages in ways described by (Angrist, 1976) for example. In general high z values for given n & p materials result in couples with a high Z.



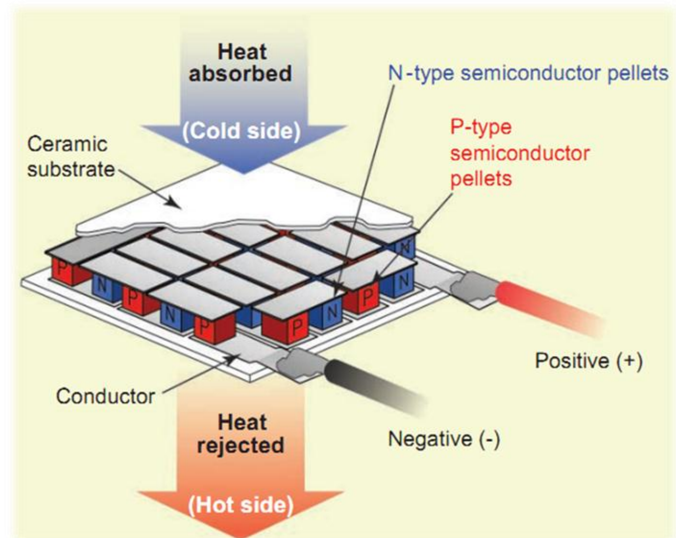


Figure 1 – Basic thermoelectric device configured in a generator mode and complete module configured as a Peltier cooler or heat pump (Bell L. E., 2008)

It is difficult to increase Z for several reasons. First, in simple materials, an increased α leads to a simultaneous decrease in σ. Adversely, an increase in σ leads to a comparable increase in κ_{el}, characterized by the Wiedemann-Franz law. So with known conventional solids, a limit is rapidly obtained where a modification to any one of the three parameters α, σ, or κ, adversely affects the other transport coefficients, so that the resulting Z does not vary significantly. Currently, the materials with the highest z are Bi_2Te_3 alloys such as $Bi_{0.5}Sb_{1.5}Te_3$, with zT ≈ 1.0 at T = 300 K. Only small increases in Z have been achieved in the last two decades, so it is now felt that the Bi_2Te_3 potential performance limit has been nearly reached. (Elsner & Ghamaty, 2005)

It has been shown that a multiple quantum well (MQW) approach results in a significant increase in z over the bulk value as the quantum-well width is decreased. The proposed increase in z arises mainly from the enhancement of the electron states per unit volume (density of states) that occurs for small well widths. The first n-type $Si/Si_{0.8}Ge_{0.2}$ and p-type B_4C/B_9C quantum well superlattices were deposited on single crystal substrates using molecular beam epitaxy (MBE) and magnetron sputtering techniques (Martin & Olsen, 2003).

SUPERLATTICE

Superlattices belong to a group of thin-film and nano-scale materials developed over the past decade that have sparked interest as candidate materials for thermoelectric devices. These include thin-film superlattices, clathrates, skutterudites, and 0 and 1 dimensional quantum-wells (Hendricks, 2005). A superlattice is, in general, a repeating pattern of two materials. For the research presented herein, the n-type superlattice is composed of alternating layers

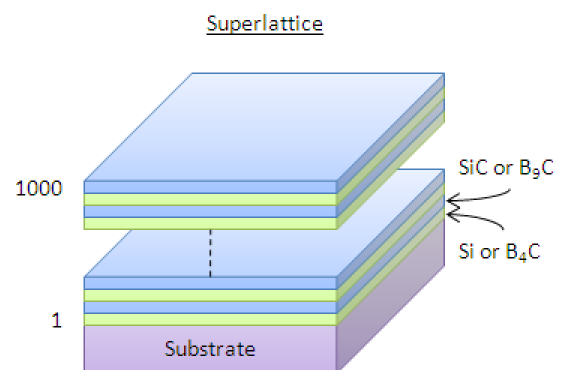


Figure 2 – Supperlatice illustration

of silicon (Si) and silicon-carbide (SiC), and the p-type superlattice is composed of alternating layers of two types of boron-carbide, B_4C and B_9C. The individual layers are typically 10 nm thick (between 1 nm and 25 nm) and can be formed into superlattices as thick as 10 μm (Ghamaty & Elsner, 2007) using 1000 layers (500 of each material). The Si/SiC superlattice has been shown to be an excellent n-type material that can operate at high temperatures, and the B_4C/B_9C superlattice is an excellent p-type material at both low and high temperatures. One particular advantage of this system is that both Si/SiC and B_4C/B_9C function as thermoelectric materials without doping. We note also that $Si/Si_{0.8}Ge_{0.2}$ is an n-type superlattice that performs well at low to moderate temperatures below 250 °C, though performance at higher temperatures has been observed to be no better than that of bulk SiGe alloys (Ghamaty, Elsner, & Bass, 2008).

ION SOURCE FOR ETCHING AND SPUTTER DEPOSITION

A broad beam ion source 8-cm in diameter was used to sputter etch (or clean) the substrate surface and then sputter target materials onto the substrate to form thin films. An ion source operates at low pressure so that the mean free path of accelerated ions is much greater than the distance between the ion source and the target or substrate surface. Figure 3 contains a sketch of a broad beam ion source. Argon gas is fed into the discharge chamber where a hot filament emits electrons to the positively biased discharge chamber walls. The plasma that is created is contained by a magnetic field, which surrounds the discharge chamber. Ions are then accelerated out of the discharge chamber by a set of positively and negatively biased grids. This accelerated beam of ions is used to sputter materials which it strikes as described in the following section. The current density of ions leaving the discharge is proportional to the beam current which is read off of the screen power supply. Furthermore the energy of the ions when they impact the target or substrate is determined by the screen voltage. A hot filament neutralizer is used to neutralize the ion beam and surfaces immersed in the ion beam. This filament emits electrons, which keep the positive ion beam from building up a charge within its volume and on

surfaces immersed in the ion beam. Were a charge to build up on the target, the impacting ion energy would be reduced, or, the ions could be prevented from impacting the surface altogether.

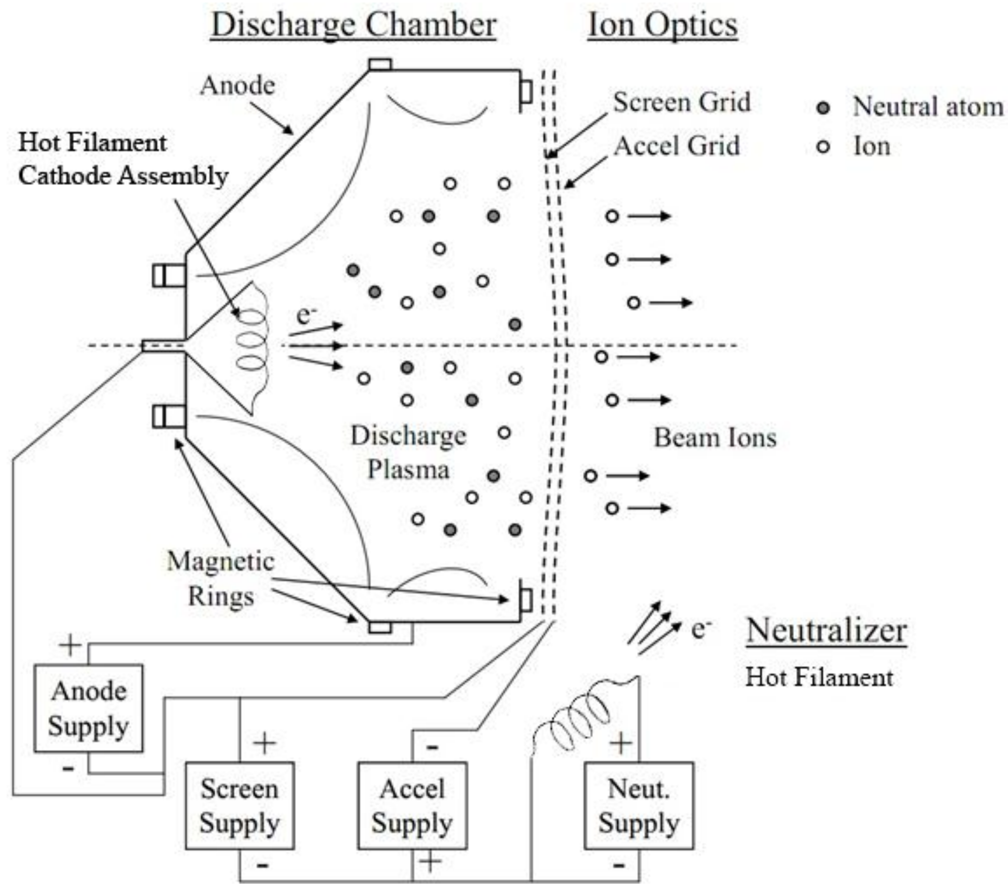


Figure 3 - Ion source (Farnell C. C., 2007)

SPUTTERING

Ion beam sputtering involves the use of an ion source to bombard a target with high velocity ions. These ions impact a target and transfer their energy to the surface resulting in structural reorganization at the atomic level and ejection of atoms off of the surface. In a low pressure environment these ejected atoms are then deposited on a substrate which views the target. Over time a thin film builds up (grows) on the substrate. Ion beam sputtering has been utilized for many decades for the deposition of high quality coatings. Using this deposition method it is possible to build thin, uniform, highly dense coatings. (Liang, Wang, & Liu, 1979)

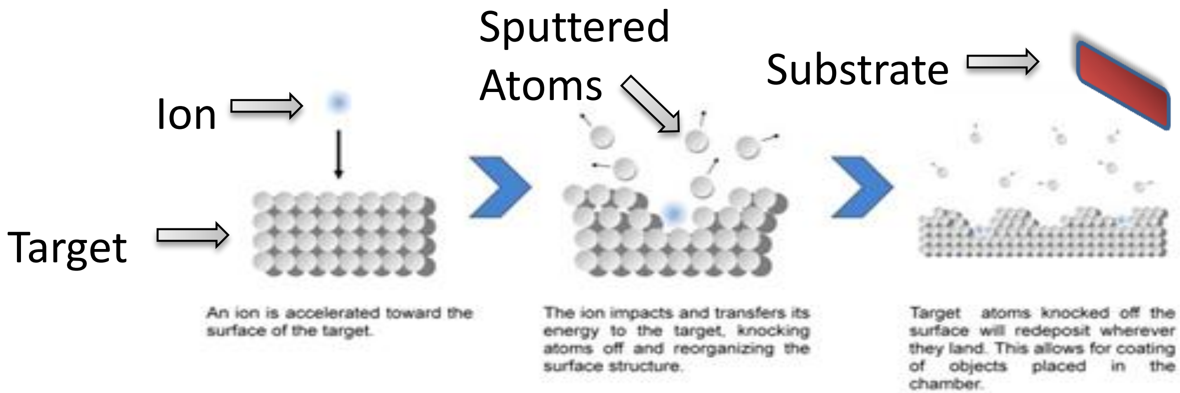


Figure 4 – Illustration of sputtering process (Riedel , 2010)

Because the sputtering process cleans and rearranges atoms on the surface of the bombarded material, ion beams can also be used to create unique textures on a surface. Etching the silicon substrate prior to depositing a superlattice film was found to enhance surface adhesion and improve the electrical resistivity of the film.

ETCHING

To etch the silicon substrates an 8cm ion source was used to create a beam of energetic argon ions. The etching rate was controlled by setting the ion energy and adjusting the rate of ions leaving the source (beam current). To ensure consistent processing, the beam current was constantly monitored and kept at 100 ± 1 mA. Height measurements of a select group of substrates were taken after processing to calculate the etch depth. Specifically, the etch rate was found using the time of etch and measuring the etch depth.

Theoretical etch rates, for comparison to the experimental etch rates, were calculated using the following assumptions: that the average ion current was 50 mA and uniform over the entire beam area, the beam diameter at the target was 16 cm (as measured from etched silhouette of the rotating platform), the density of the silicon was 2.33 g/cm^3. (Yamamura & Tawara, 1996) The equation used for the calculations is shown in Equation 3

Equation 3 – Etch rate

$$Etch\ Rate\ = \frac{\mathrm{Y \cdot j \cdot m}}{\rho \cdot e}$$

Y: Sputter Yield (atoms/ion)

j: Ion Current Density (C/m^2s)

m: Mass of Silicon Atom (kg/atom)

ρ: Density of Silicon (kg/m^3)

e: Elementary Charge (C)

These calculations led to a predicted etch rate of 1.2 nm/s, while the measured etch rate for silicon was 1.1 nm/s. Etch times were typically 15min which resulted in ≈1µm etch depth. This is a significant difference between magnetron systems as their low energy ions are unable to effectively etch substrates.

QUANTUM CONFINEMENT WELLS

An ideal thermoelectric material behaves like an electron-crystal, phonon-glass (Snyder & Toberer, 2008). The ideal material avoids scattering electrons, to maintain high electrical conductivity, while scattering phonons to reduce thermal conductivity to prevent excessive heat flow. Phonons have varying wavelengths and mean free paths, from less than 1 nm to greater than 10 µm, and therefore scattering at multiple length scales is desired to minimize thermal conductivity.

Here, we are most interested in the case where the heat flux and electrical current are parallel to the film. The net quantum well effect can be summarized as follows: the Seebeck coefficient is increased due to an increase in the density of states, the electrical conductivity is increased due to enhanced mobility of the carriers, and thermal conductivity is reduced due to phonon scattering at the QW layer interfaces. (Jovanovic, Krommenhoek, Ghamaty, & Bass, 2007)

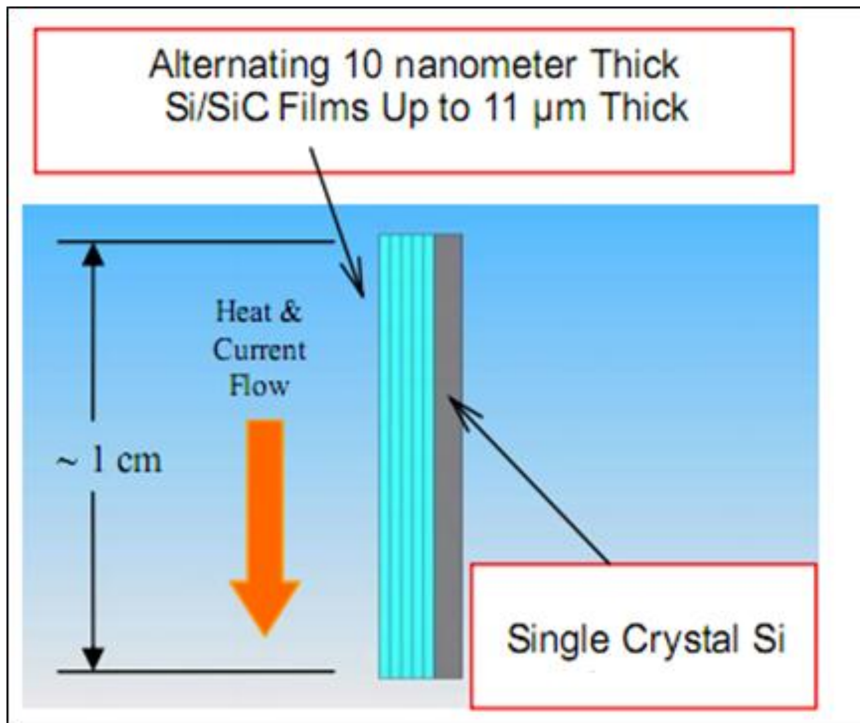


Figure 5 – Thermoelectric device – heat and current flow parallel to layer direction (Jovanovic, Krommenhoek, Ghamaty, & Bass, 2007)

EXPERIMENTAL SETUP, METHODS AND DIAGNOSTIC TOOLS

VACUUM FACILITY

The vacuum chamber, illustrated in Figure 6, houses the ion source, targets and substrate holder. The vacuum chamber is “pumped down” and maintained at low pressure via two pumps. The first is a mechanical pump which is attached to the chamber through a pneumatically operated valve. This pump reduces the chamber pressure to 15 – 20 Pa. At this point the valve is closed and the mechanical pump is switched off. Next a second, larger pneumatically operated gate valve is opened to connect a Cryo-pump to the main chamber. With a good seal base pressures of 2.0×10^{-4} Pa (~1.5×10^{-6} Torr) are achieved. During ion source operation the chamber is typically at pressures of 5.0×10^{-3} Pa (~3.8×10^{-5} Torr) due to the flow of argon used to operate the source.

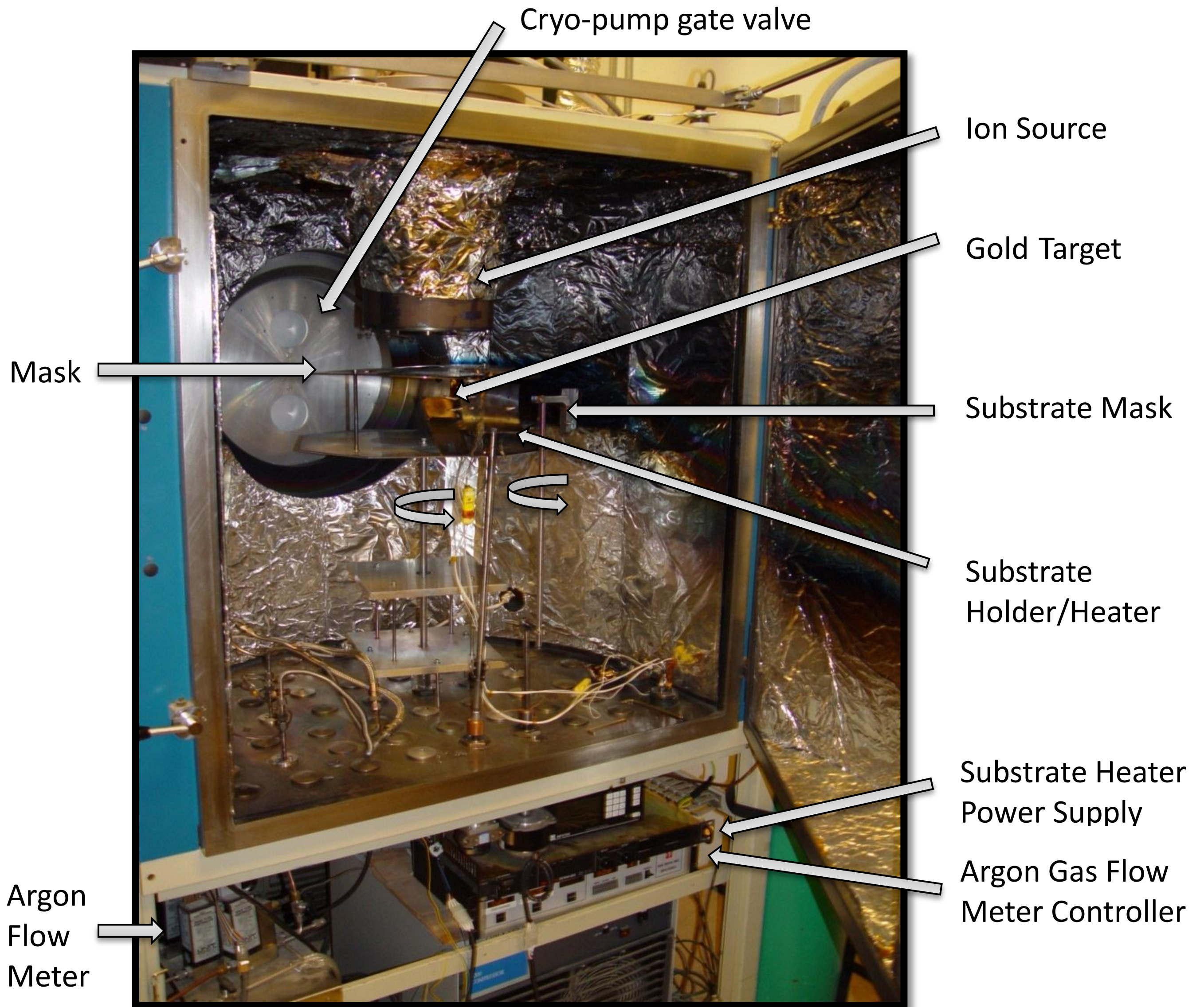


Figure 6 – Vacuum chamber (gold deposition configuration shown)

THIN FILM DEPOSITION CONFIGURATION

The deposition system was designed to deposit alternating thin, on the order of 10 nm thick, layers onto planar substrates to form superlattice films. Three major components make up the thin film deposition system. First, the ion source served as a source of energetic particles used to either sputter target materials or etch substrates. Second, sputter targets were arranged to provide the necessary materials

for deposition. Finally, the substrate holder both held and heated the substrate to facilitate improved film properties.

ION BEAM CONFIGURATION

The ion source is oriented vertically and can be seen in Figure 7. The benefit of this vertical orientation is that it allowed the use of low-cost powder-based targets. In other systems, targets may need to be held vertically, preventing the use of powder targets. With the vertically mounted source, the targets were held at an angle of 45° with respect to the ion beam to increase sputter yields (the targets are shown at 0° relative to the ion beam in Figure 7), while keeping the powder contained in the holding tray.

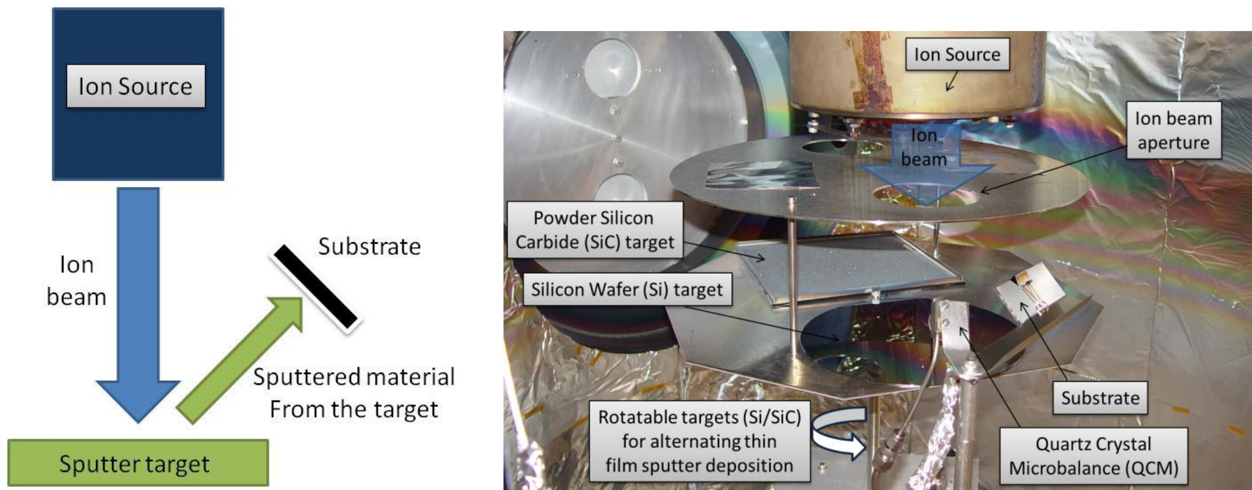


Figure 7 - Diagram and picture of the thin film deposition setup

Alternating thin film layers were deposited onto a substrate by ion beam sputtering of selected target materials. Computer controlled stepper motors were used to alternately rotate the targets into the ion beam. Deposition rates were monitored using a QCM placed nearby the substrate.

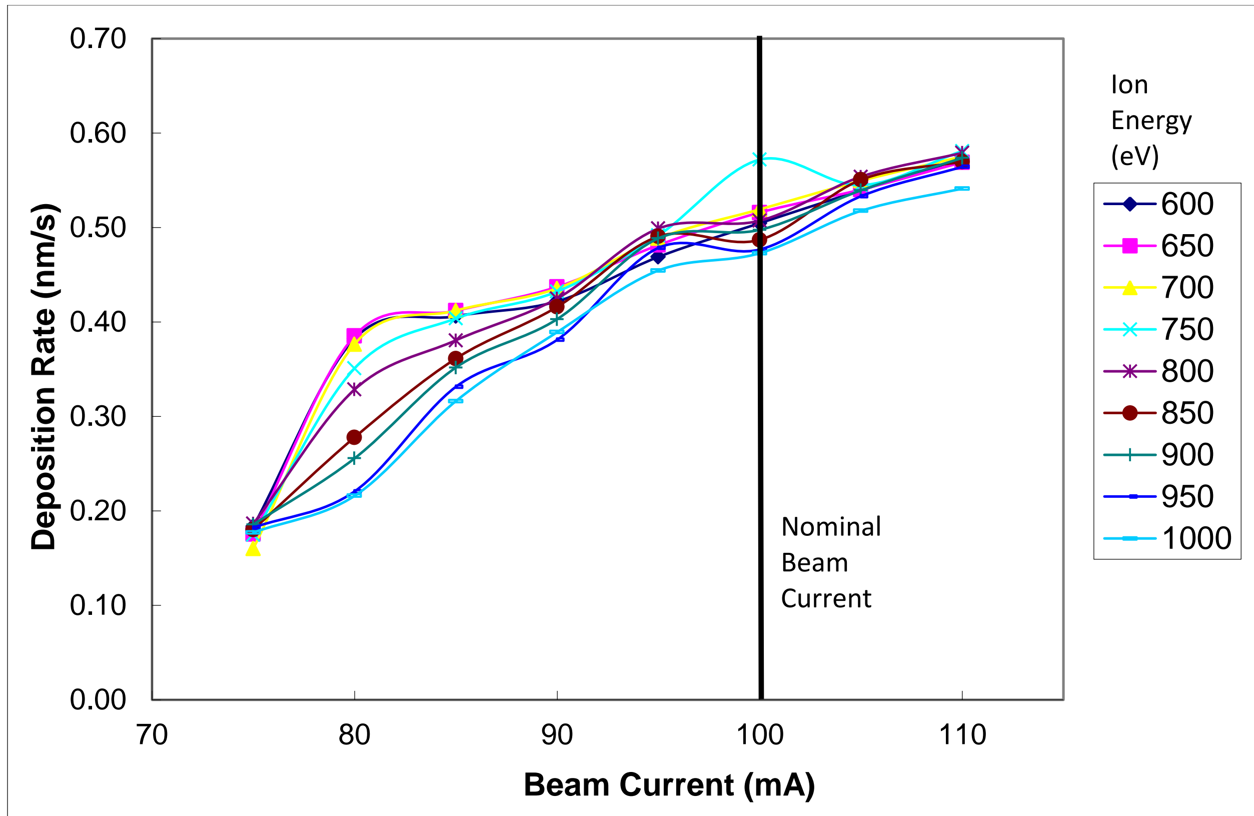


Figure 8 – Beam current vs. deposition rate at various ion energies for a Si wafer target

The deposition rate increases with ion current densities as well as the energy of the ions.

TARGET AND MASK CONFIGURATION

One of the major obstacles is determining an efficient method for laying films of alternating composition while avoiding contamination. For example for the n-type superlattice silicon and silicon carbide were used in alternating layers. In order to deposit these layers a method was developed to switch targets. This was done using a rotating tray with two distinct locations for either target. This apparatus is shown in Figure 7. In this photograph the silicon target is placed under the ion beam and is being deposited. When the desired thickness is reached the tray will rotate and silicon carbide be placed under the ion beam. A mask is used between the source and sputter targets to selectively sputter only one material at a time. To further prevent contamination a second retractable mask was used between the sputter

targets and the substrate. When the desired thickness is reached the mask closes and does not re-open until the tray has completely rotated to the new location.

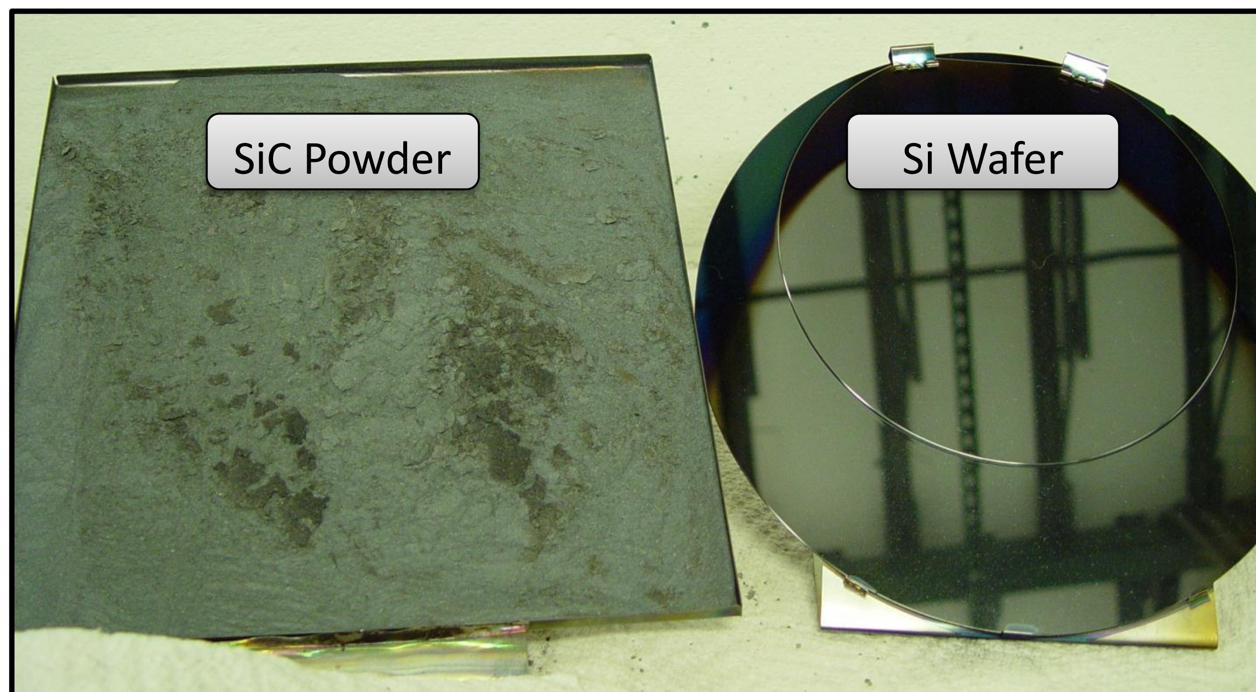


Figure 9 – Sputter deposition targets: SiC powder and Si wafer respectively

SUBSTRATE HOLDER CONFIGURATION

The silicon carbide shown in Figure 9 was purchased from Alfa Aesar and has 99% purity. Clean uncontaminated powder was used for each run in order to ensure other material particles had not infiltrated the powder. The silicon wafer is comprised of a smaller diameter n-type phosphorus (Ph) doped wafer on top and a larger diameter p-type boron (B) doped wafer on bottom. This configuration was used due to the high cost of intrinsic silicon. The purity is greater than 99.9% and useful as an insulator due to the high resistivity.

To maximize deposition rates the substrate was placed at a 90° angle relative to the direction of the beam, this corresponds to a 45° angle relative to the plane of the sputter targets. Samples were mounted to the holder via stainless steel shims, which served a dual purpose in providing a mask for a

portion of the substrate. For gold deposition, which will be discussed later, the masks were moved to cover the superlattice and facilitate the gold contact deposition.

The substrate holder contained a heater. Tests were performed at various temperatures during deposition and after deposition for annealing the film. Temperatures from 200°C to 800°C could be achieved.

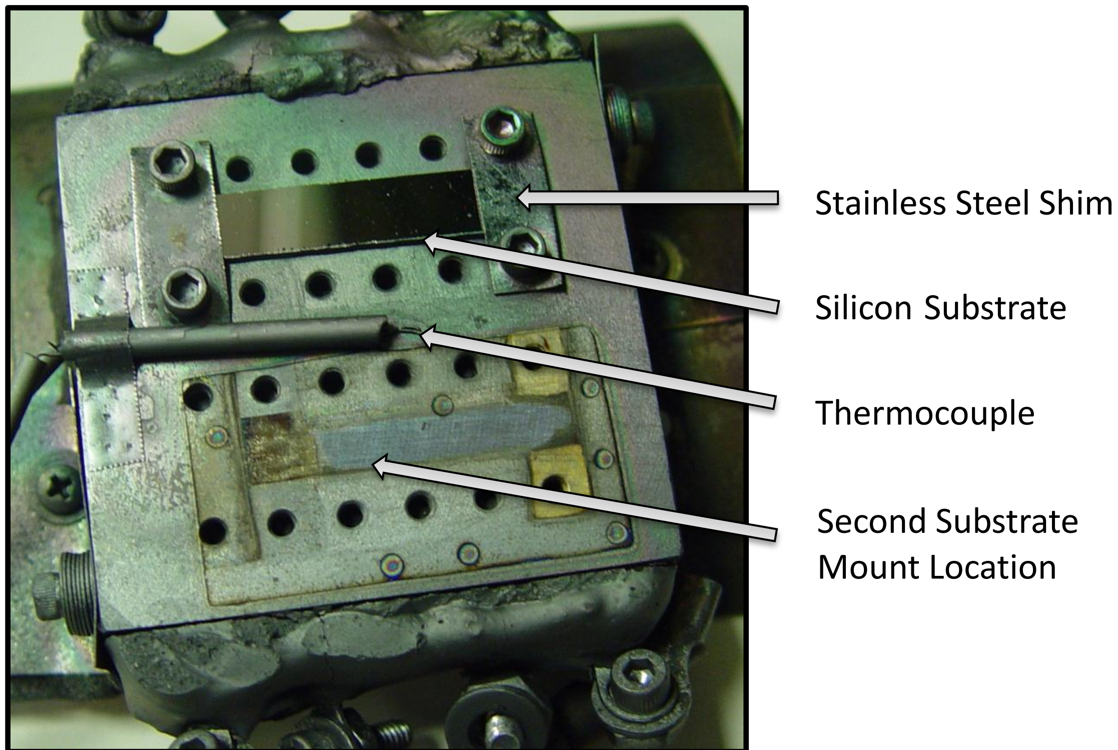


Figure 10 – Substrate holder/heater

A thermocouple was attached to the outside of the heater in order to verify power curves and monitor the deposition temperature. The obvious error in this measurement is that the surface of the silicon being deposited may not be the same temperature as the surface of the heater. A fluent analysis was performed in order to determine if the conduction through the silicon resulted in a similar temperature to the heater. Ultimately the results showed a 3°C drop from heater surface to silicon surface. This

change was taken into account for all heater temperatures. The resulting 3D temperature curve from the Fluent analysis can be seen in Figure 11.

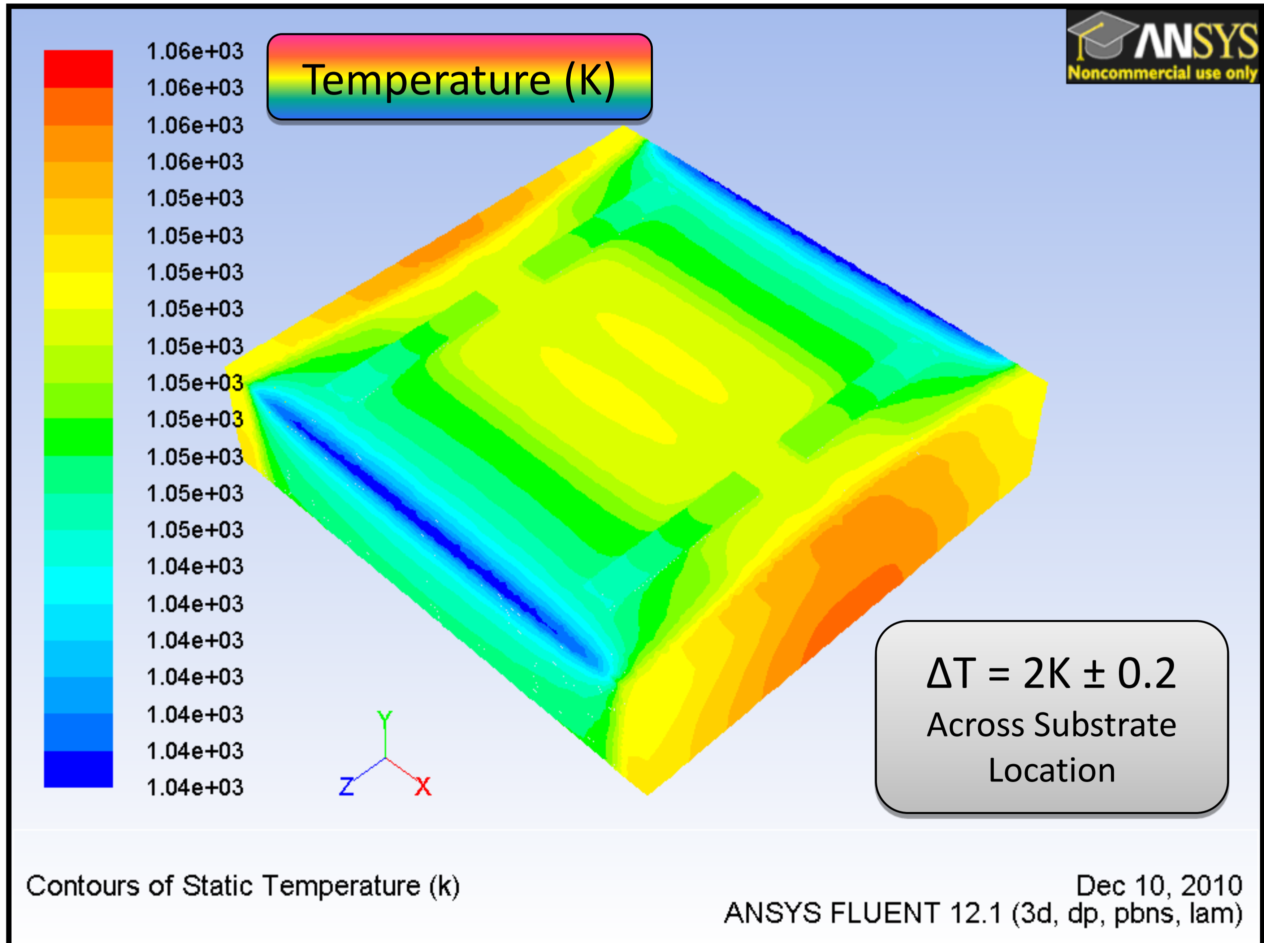


Figure 11 – Fluent substrate surface temperature analysis

DEPOSITION AUTOMATION

The entire deposition and substrate temperature control process has been completely automated. The target platform rotation and the substrate mask retraction are controlled via stepper motors. These motors are monitored via Labview and motion is triggered using the QCM. Furthermore, the ion source settings are monitored and controlled via Labview, which ensures a consistent beam current and uniform deposition rate.

Typically, 60 alternating layers of either Si/SiC or B_4C/B_9C are laid down on each substrate. Substrate temperature was controlled using thermocouples placed behind the silicon substrate. Once the layers were deposited, gold electrical/thermal contacts were sputtered onto each end of the superlattice for performance evaluation using a mask to shield the center section of the superlattice from being coated. This process allowed evaluation of the electrical conductivity and Seebeck values.

The deposition process was automated using LabView software. The ion source was monitored and controlled through RS-232 communication. The thickness of each layer was monitored using the QCM, whereby a mask was applied after the desired thickness was reached.

A typical deposition was performed at 500 °C, with some samples deposited at 200 °C.

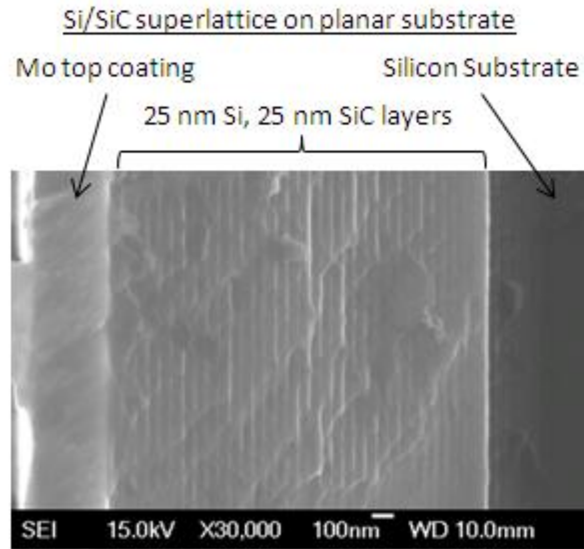


Figure 12 – SEM image Si-SiC superlattice

DEPOSITION SYSTEM AUTOMATION

The beam was current was maintained at ±1 mA of the desired current. In addition the neutralizer emission current was also maintained within 1mA. These values were logged over the course of the run to ensure there were no significant changes while processing. A sample data set of the beam and neutralizer emission current over time can be seen in Figure 13.

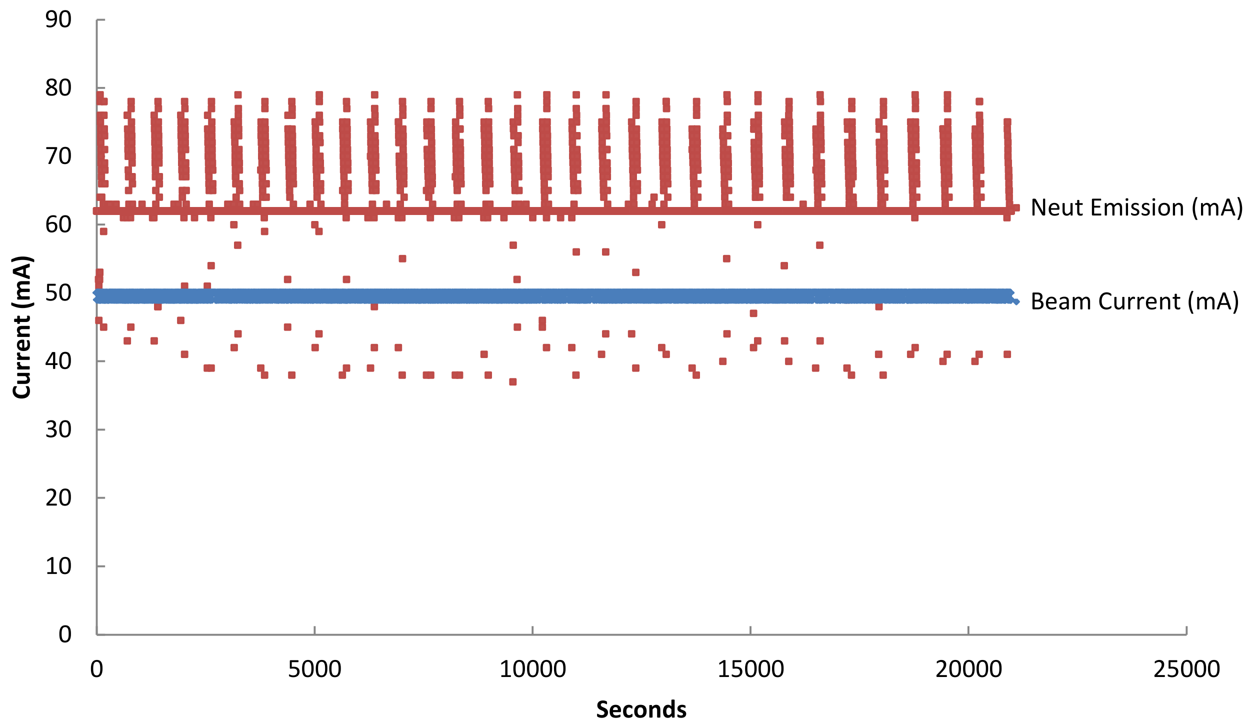


Figure 13 – Beam current and neutralizer emission current during a 50 mA deposition – the increases in neut current are due to the deposition setup rotating between targets.

QCM CONFIGURATION

A Quartz Crystal Microbalance was used to monitor layer thickness during deposition. The QCM was oriented so as to be at the same height and angle as the substrate. By monitoring the change in mass of the QCM's crystal the layer thicknesses could be determined. These measurements were later correlated to layer/film thickness using white light interferometry to ensure accuracy. Cooling lines were also attached to the QCM to maintain a steady temperature.

In the ion beam deposition system, rates of 30 nm/min for Si and 10 nm/min for SiC, and 1 nm/min for both B_4C and B_9C were achieved. This compares to 6 nm/min and 36 nm/min for Si and $Si_{0.8}Ge_{0.2}$ layers and 0.8 nm/min for boron carbide (B_4C) films published elsewhere using magnetron sputtering (Martin & Olsen, 2003). More recently, deposition rates of 10 nm/min were claimed for Si and $Si_{0.8}Ge_{0.2}$ layers

using magnetron sputtering sources (Leavitt, Krommenhoek, Ghamaty, & Elsner, 2010). Higher rates of deposition can be achieved with ion beams when higher ion energies are used.

ION BEAM ADVANTAGES

In this work, the ion beam system led to deposition rates comparable or slightly better than those of magnetron systems published in the literature, though it is understood that it is difficult to directly compare system geometries and operating conditions. The ion source was found to be particularly advantageous for sputtering both solid and low-cost powder sputter targets, and for etching the silicon substrates. The ability to change beam current and ion energy was found to be very useful for studying their effects on deposition and etch rates.

SEEBECK MEASUREMENT

To measure the Seebeck coefficient, the sample was placed in a heated furnace with one side of the substrate attached to a cooled rod. The cooled rod allowed a temperature difference to be created across the sample, typically on the order of 15°C. The Seebeck coefficient was calculated by measuring the temperature difference, the thermoelectric current produced by the sample, and the sample resistance:

Equation 4 – Seebeck coefficient

$$\alpha = \frac{\Delta V}{\Delta T}$$

Where:

Equation 5 – Voltage

$$\Delta V = \frac{I}{R}$$

Here α is the Seebeck coefficient, T is temperature, I current and R resistance.

The following measurements were taken consecutively using a data acquisition device. First the thermoelectric current was measured, then two temperature measurements were taken using platinum RTDs, finally the resistance of the sample was measured using a 4-point resistivity measurement. All measurements occurred within 1/10th of a second. From these three measurements the Seebeck coefficient could be determined using Equation 4 and Equation 5. In order to improve upon the temperature measurement uncertainty, an infrared (IR) camera was used to display the temperature difference generated across the sample.

RESISTIVITY MEASUREMENT

To measure the electrical resistivity as a function of temperature the superlattice was placed within an air furnace. At selected temperatures, a 4-point resistivity measurement was performed by applying a known voltage across the film and measuring the resulting current. The temperature was measured at two locations on the sample. All measurements were done using platinum RTDs (±0.3°C) to measure temperatures up to 500°C. These measurements were verified visually using an IR camera. The temperature difference across the sample was typically 10-15°C. The resistivity was then found by:

Equation 6 - Resistivity

$$\rho = R\frac{A}{l} = \frac{V}{I}\frac{wt}{l}$$

Where ρ is the resistivity, R is the measured resistance of the sample, A is the cross sectional area of the sample (which is measured during deposition by a quartz crystal microbalance (QCM)), and l is the length of the sample. Typically, films contained 60, 10-nm layers, for a total of 600 nm thickness. The length and width of each sample was measured after deposition. All of these measurements were verified using a white light interferometer.

THERMAL CONDUCTIVITY MEASUREMENT

Working in collaboration with Dr. Barry Zink at University of Denver a low-stress silicon-nitride beam was used to measure thermal conductivity. A typical Si-N beam is shown in Figure 14.

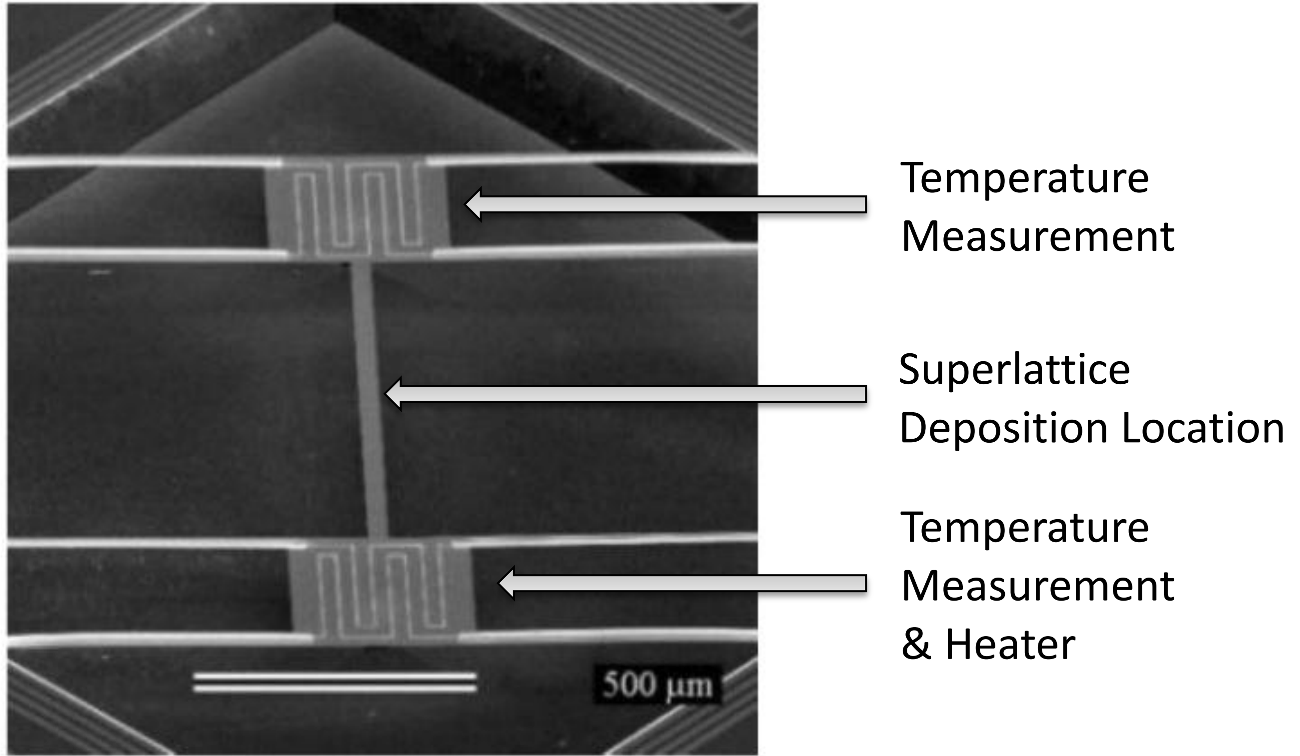


Figure 14 - Two Si–N islands connected together by an 806 µm long, 35 µm wide, and 500 nm thick Si–N suspended beam (Sultan, Avery, Stiehl, & Zink, 2009)

DATA AND RESULTS

THICKNESS MEASUREMENTS USING WHITE LIGHT INTERFEROMETERY

A total of four (4) materials were deposited on pure intrinsic silicon (Si) which served as the substrate. Deposited or target materials included pure silicon, silicon carbide, boron B_4C carbide and boron B_9C carbide. The deposition rates of all of these materials needed to be characterized to control film thickness. This was first done via QCM monitoring, whereby the mass deposited on the QCM was measured and using the material density the thickness was determined. However, it is known that the density of sputtered materials often varies from that of bulk materials (Liang, Wang, & Liu, 1979); furthermore the QCM location was slightly offset from the substrate resulting in another small variance. These factors were taken into account and a correction factor was applied to achieve an accurate desired thickness. This was then verified using white light interferometry and final corrections were made. Final corrections were typically less than ± 5% or 5 Å for the 10nm layers. As mentioned previously step differences were created by placing stainless shims over selected regions of the substrate to mask deposition over these regions. Figure 15 shows a typical SWLI data set for a Si film; the deposition time was extended to obtain a thicker film and allow more accurate measurements to be made.

Table 1 – Correction factors due to white light interferometry verification

	Silicon	Silicon Carbide	$Boron_4Carbide$	$Boron_9Carbide$
Expected Thickness (nm)	100	100	100	100
Measured Thickness (nm)	129	117	50	47
Correction Factor	1.29	1.17	0.50	0.47

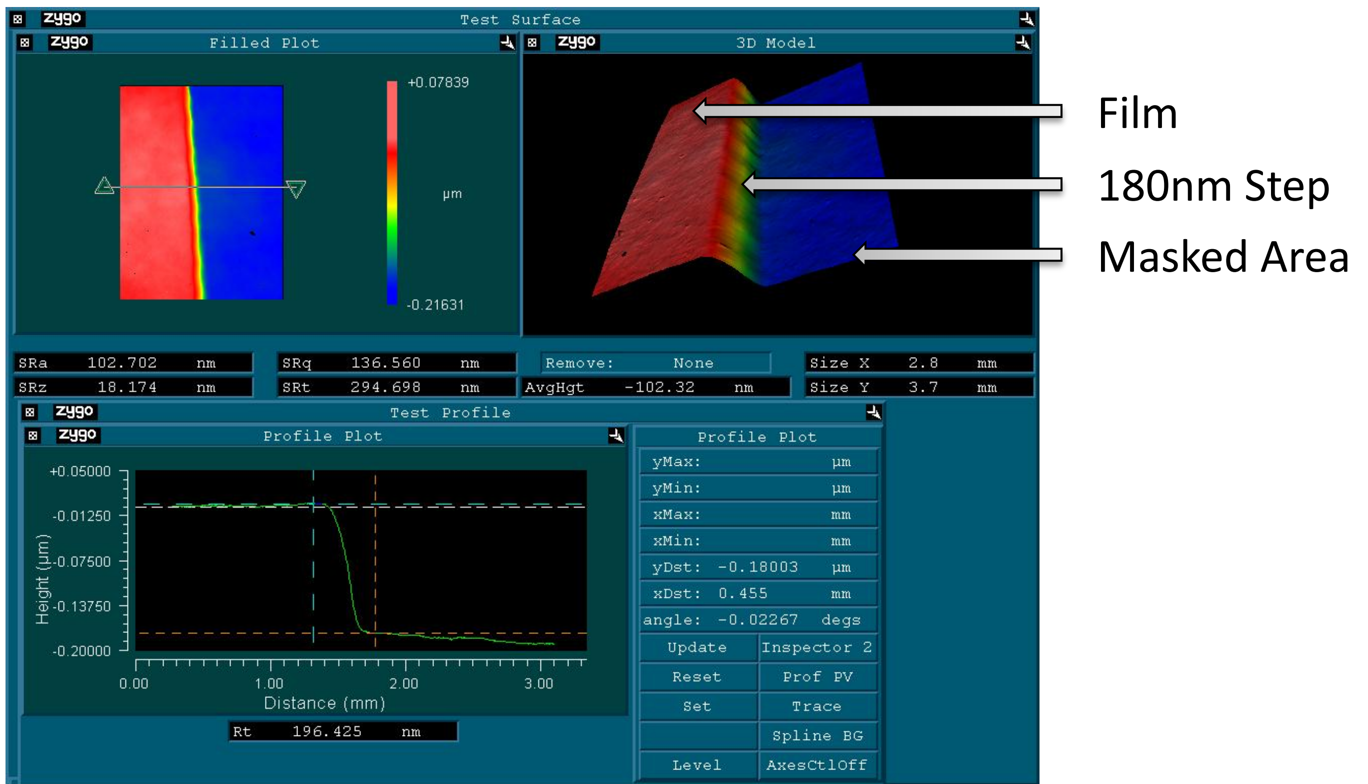


Figure 15 – White light interferometer step height data. The film was found to be 180.0 nm thick with a standard deviation of ± 2 nm.

EFFECTS OF TEMPERATURE ON FILM QUALITY

A substrate heater was installed primarily to combat film adhesion issues. It was found that at temperatures in excess of 400°C, stress relief was achieved and films remained well adhered to the substrate. An example of film delamination can be seen in Figure 16 and Figure 17.

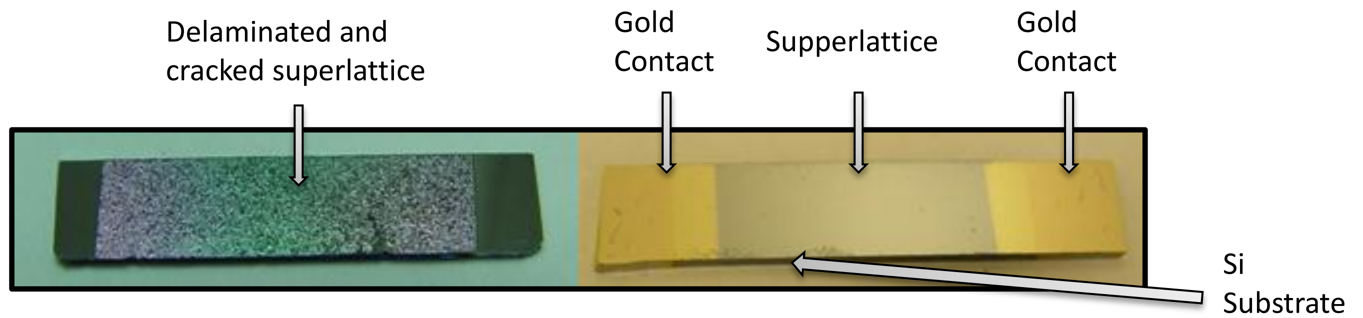


Figure 16 – Sample deposited at 200°C (Left) shows significant delamination and cracking compared to sample deposited at 500°C (Right) note that gold contacts have been deposited.

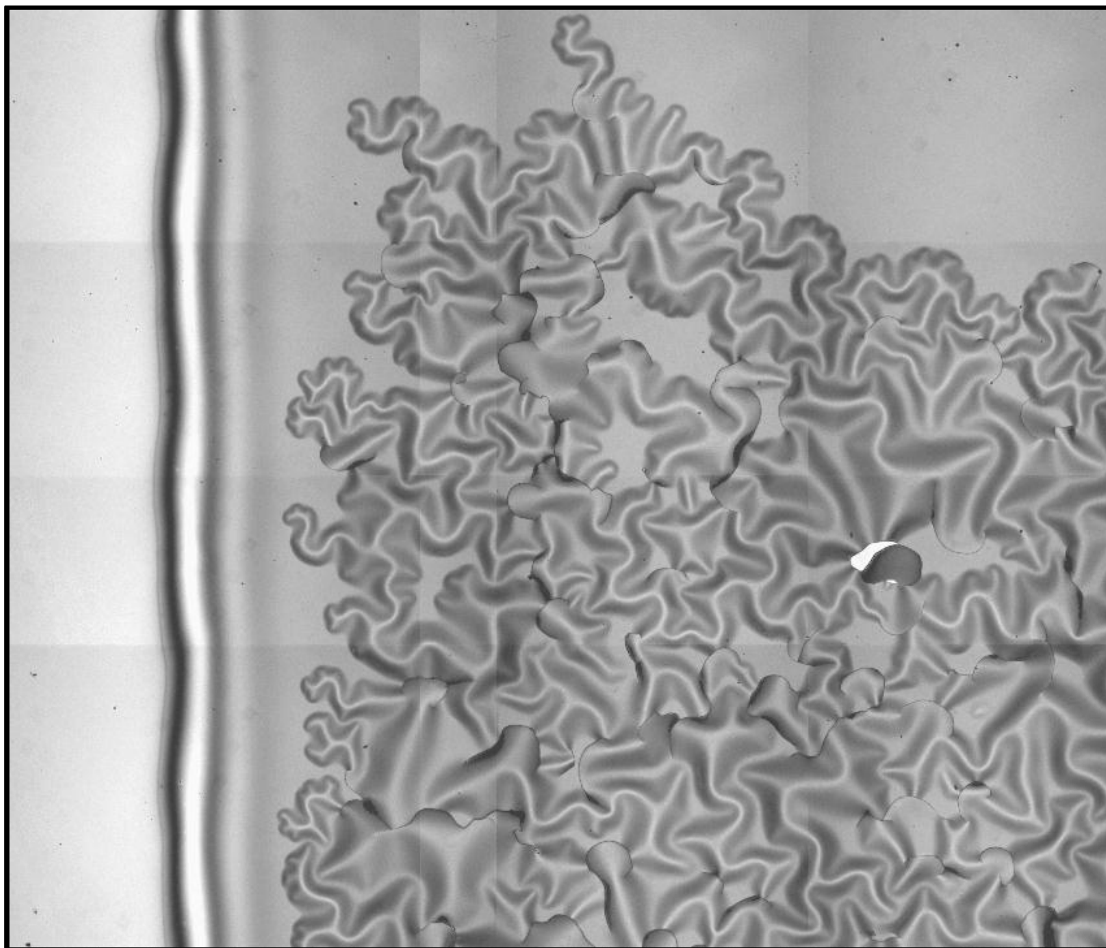


Figure 17 – SWLI intensity map showing film delamination due to film stresses – deposited at 200°C

SI-N BRIDGES

University of Denver produced micro-machined Si-N bridges that were used as a substrate on which the superlattice film was deposited in order to measure thermal conductivity. The bridges were first characterized in the white light interferometer to ensure proper film deposition could be achieved.

OVERVIEW

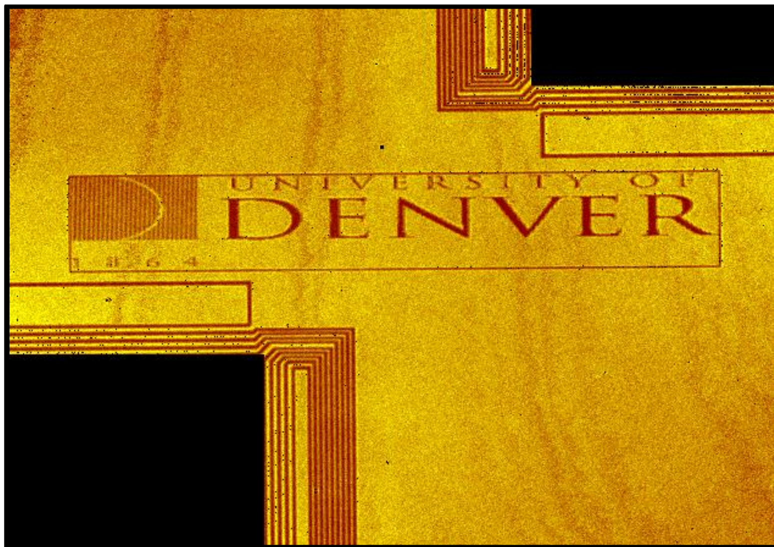


Figure 18 - University of Denver logo on Si-N bridge-wafer approx. 2.36mm wide

As shown in Figure 19, the overall form of the bridge is bowed. The average difference in height between the highest point located on the connection and lowest point on the Si-N bridge is 11.07 ± 0.1µm. Although not flat, the extent of the deflection of the bridge is small and does not affect the superlattice deposition process.

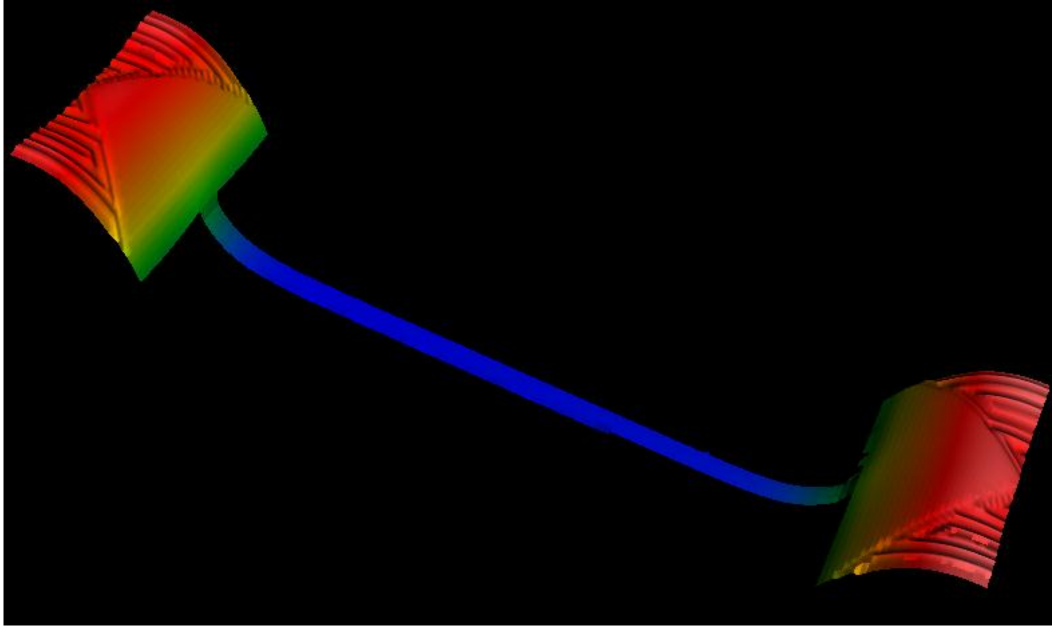


Figure 19 – Si-N bridge form approx. 11µm height, 1mm length

Figure 20 shows the roughness of the Si-N bridge to be 1.0 ± 0.1 nm.

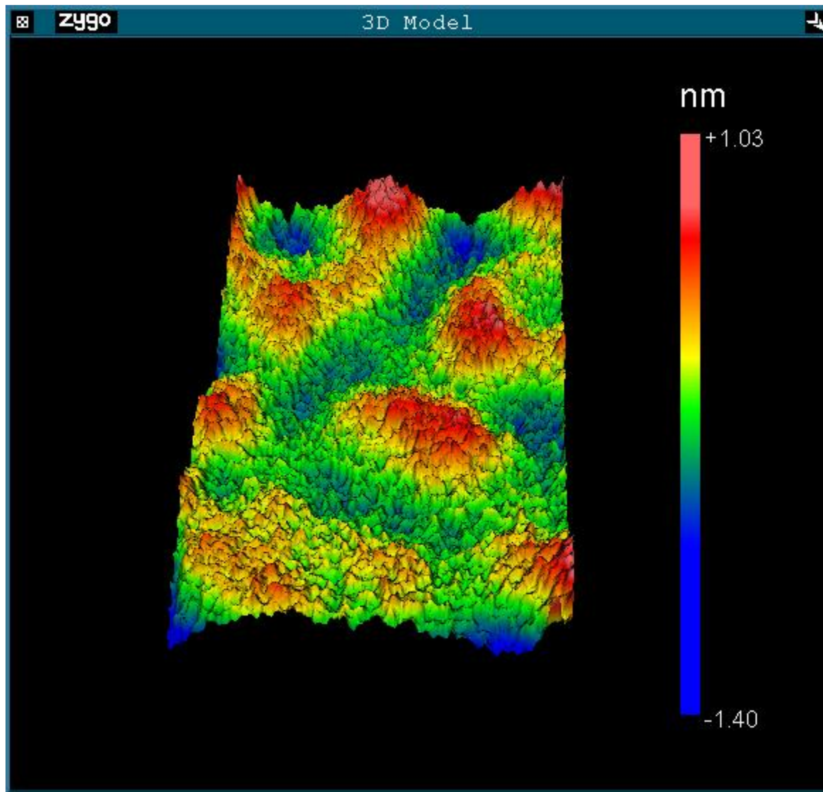


FIGURE 20 – SI-N BRIDGE ROUGHNESS

Figure 21 shows the side-to-side curvature of the bridge. It should be noted that this corresponds to a maximum angle relative to flat of 0.162 ± 0.01° and a total vertical deflection of 22.6 ± 1nm, which is much less than the deflection along the length of the bridge.

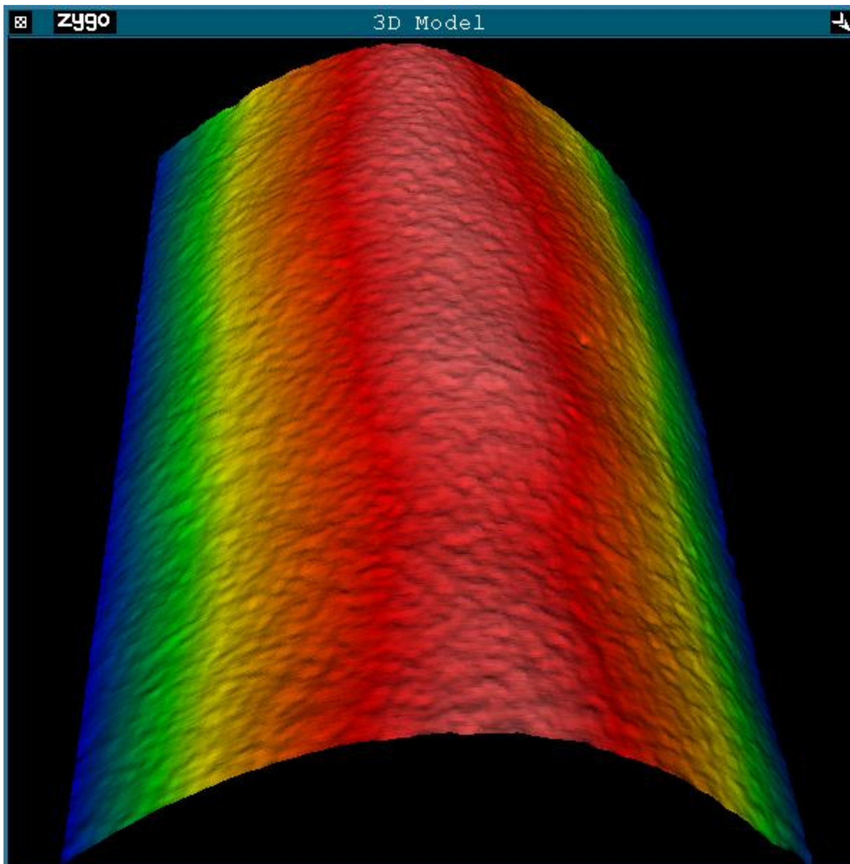


Figure 21 – Si-N bridge curvature

Figure 22 shows the step junction between the connection point and the electrical leads that are deposited on the Si-N bridge. This step is 309.3 ± 2.3nm in height.

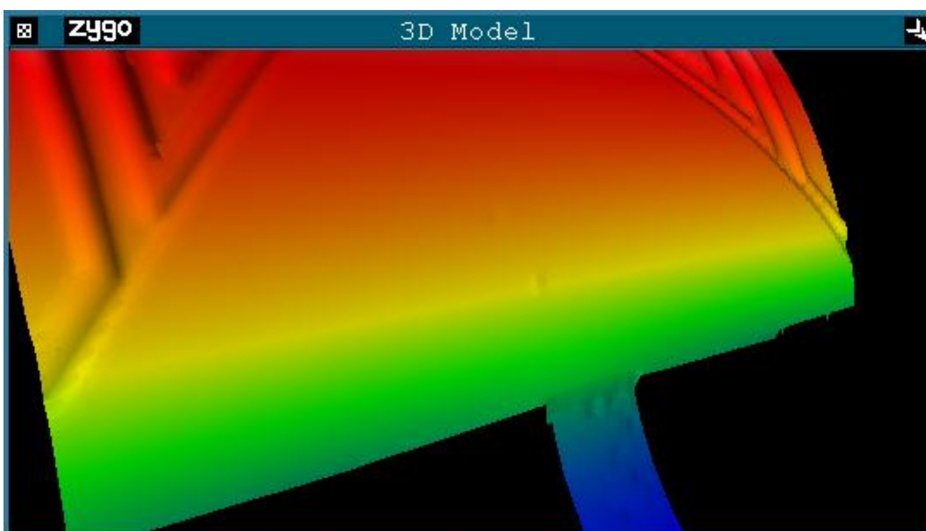


Figure 22 – Si-N electrical contact

MEASUREMENTS

Etch rates were determined by etching a blank Si-N sample for different lengths of time at constant energy. From this, the etched step height was measured using SWLI and a resulting etch rate was determined. Furthermore the roughness was measured to determine the role of roughness on both film adhesion and thermoelectric properties.

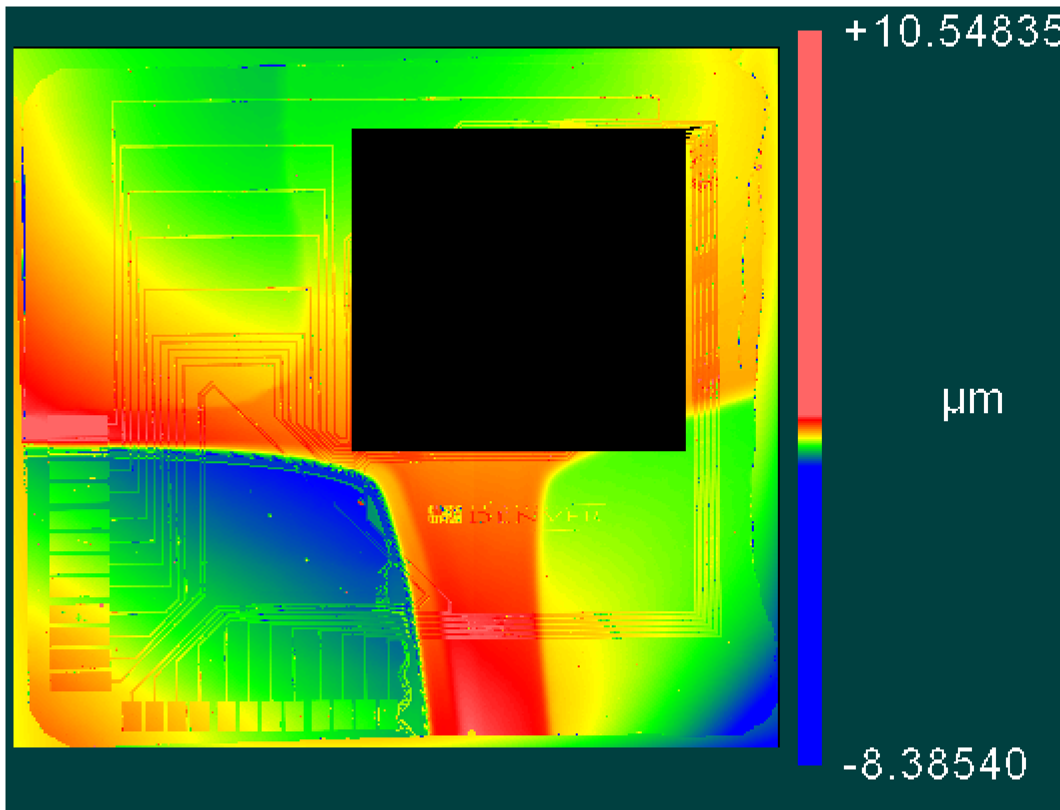


Figure 23 – WLI image showing varying etch times on Si-N, 1200V beam voltage, 100mA beam current:

Top Left: 1 min etch time
Top Right: 0 min etch time
Bottom Left: 15 min etch time
Bottom Right: 5 min etch time

ROUGHNESS AND RESISTIVITY

The silicon substrates, upon which the films were deposited, were purchased in a lapped condition, and had an initial surface roughness of 0.92 nm. The silicon substrates were etched using ion beam bombardment to remove any residual surface contaminants to ensure good film adhesion. Following etching, the average surface roughness increased to 1.16 nm. The results of substrate etching are listed

in Table 2. It was found that the resistivity of films on etched substrates was significantly lower, and therefore better, than the resistivity of films on un-etched substrates. Further, the resistivity of films deposited at 500 °C was consistently lower than those deposited at 200 °C, presumably due to a higher crystallinity of the silicon layer from in-situ annealing. In comparison to literature data, quantum well structures with high electrical conductivity and Seebeck coefficient were deposited at substrate temperatures of 400°C (Si/SiGe) and 500°C (B_4C/B_9C) (Martin and Olsen 2003).

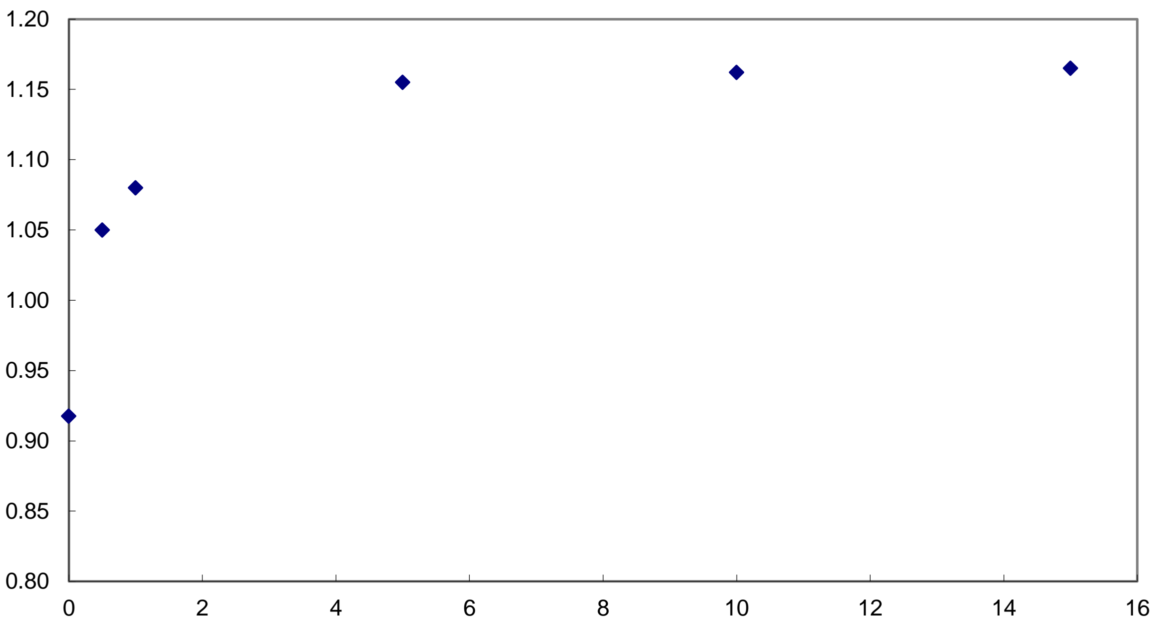


Figure 24 – Substrate surface roughness as a function of etch time. The substrates were etched using 1200 eV argon ions.

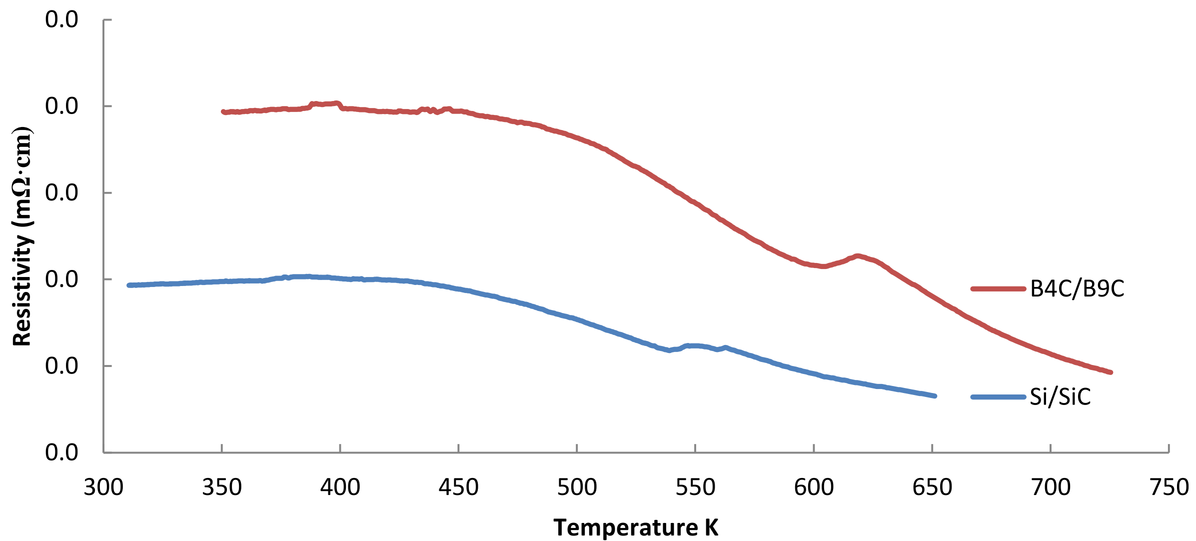


Figure 25 – Resistivity as a function of temperature of 60 layer, 10 nm per layer superlattices deposited at 500°C

Table 2 – Silicon/Silicon Carbide lattice depositions

Test Date	Number of Layers	Individual Layer Thickness Si/SiC nm	Film Thickness nm	Resistivity mΩ-cm	Etched Substrate	Deposition Temperature °C
1/4/11	60	18/13.4	942	1.1	Yes	200
1/4/11	60	18/13.4	942	1.3	Yes	200
1/5/11	60	14.8/8.8	708	0.5	Yes	500
1/5/11	60	14.8/8.8	708	0.8	Yes	500
3/2/11	34	10/10	340	148	No	500
3/2/11	34	10/10	340	204	No	500
3/8/11	60	10/10	600	0.9	Yes	500
3/8/11	60	10/10	600	1.4	Yes	500

Notes: Two samples were deposited simultaneously. 60 layers is 30 layers of Si and 30 layers of SiC for example.

SEEBECK COEFFICIENT MEASUREMENTS

The Seebeck Coefficient is measured using the same air furnace and electrical contacts with a few minor changes. First, a temperature difference needs to be created across the sample. Using a cooling rod, a temperature difference of ≈15 °C was created across the sample. By measuring the temperature difference and the thermoelectric current produced by the sample as described earlier, the Seebeck

coefficient was calculated. As part of the Seebeck calculation, it is necessary to know the resistance at a particular temperature. This resistance is known from the four-point resistivity measurements. Like resistivity, the Seebeck coefficient is also measured as a function of temperature. There tended to be a 25% uncertainty in the Seebeck coefficient measurements due to the accuracy at which the temperatures were known.

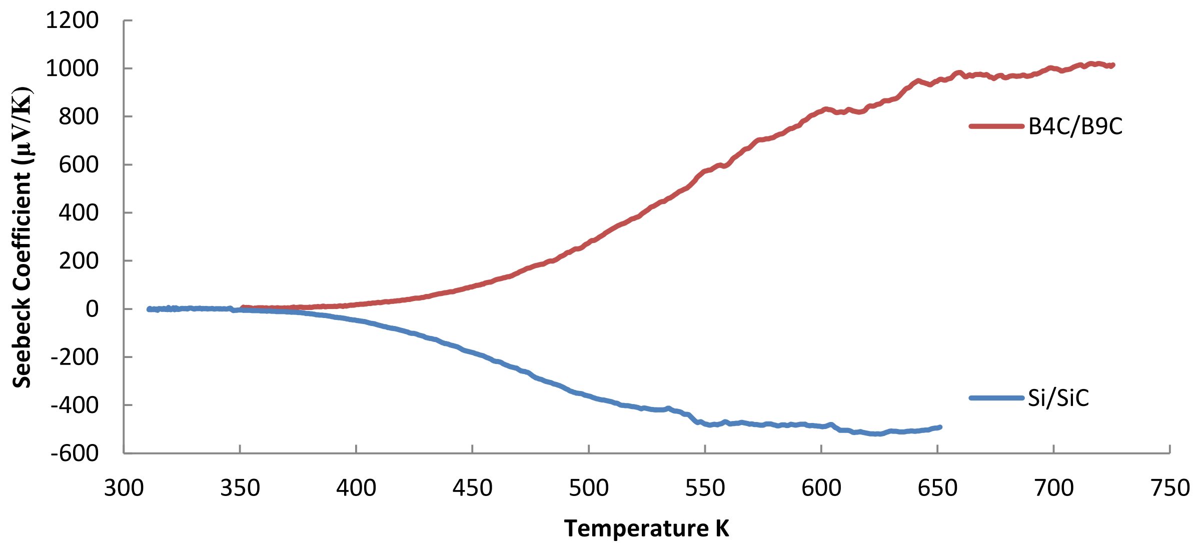


Figure 26 – Seebeck Coefficient as a function of temperature of 60 layer, 10 nm per layer superlattices deposited at 500°C

THERMAL CONDUCTIVITY

The University of Denver team first analyzed and then provided a Si-N bridge for thin film deposition. A 60-layer, 600-nm, Si/SiC superlattice was deposited onto this bridge and returned to DU for analysis. Figure 27 shows the thermal conductance in nW/K of both the Si-N bridge before multilayer deposition (green circles) and after the 600-nm Si/SiC thin film was deposited on the bridge (blue circles). The thermal conductivity of the film (in the in-plane direction) is determined by subtracting the background (substrate) conductance from the total conductance, then scaling for the film geometry. The resulting

thermal conductivity is shown in the right graph of Figure 27 (blue circles), where the units are $\frac{mW}{cm \cdot K}$ (divide these by 10 to get $\frac{W}{m \cdot K}$).

There are two estimated upper limits also shown on the thermal conductivity figure. The first, labeled "Realistic Upper Limit" assumes that deposition of the film caused a 15% drop in the conductance of the Si-N bridge. Over the last several months, Prof. Zink's group has been investigating in detail what they believe is a relatively small change in the bridge conductance that sometimes occurs after film deposition, which is currently believed to be a result of changes in surface scattering. They observe a reduction of conductance of usually only a few percent. The "Realistic Upper Limit" is therefore most likely an overestimate of the worst-case scenario caused by this surface effect. The "Unphysical Upper Limit" assumes that the entire thermal conductance measured after film deposition was through the 600 nm thick multilayer film. There is no scenario or reason to believe that this occurred, but it does provide the largest possible estimate of film thermal conductivity based on the data.

At all temperatures, the measured thermal conductivities were significantly lower than expected (below 0.7 W/(mK)) even considering possible changes to the platform's conductance following deposition.

The thermal conductivity is very low and good for a potential thermoelectric material. The thermal platform is designed to allow measurements of Seebeck and electrical conductivity (in addition to thermal conductivity) on the same thin film sample. However, a problem with the electrical leads on this particular platform unfortunately prevented DU from making the necessary electrical measurements. Future work would involve a more complete measurement by DU. It is noted that the thermal conductivity was measured at temperatures below 340K (<67°C).

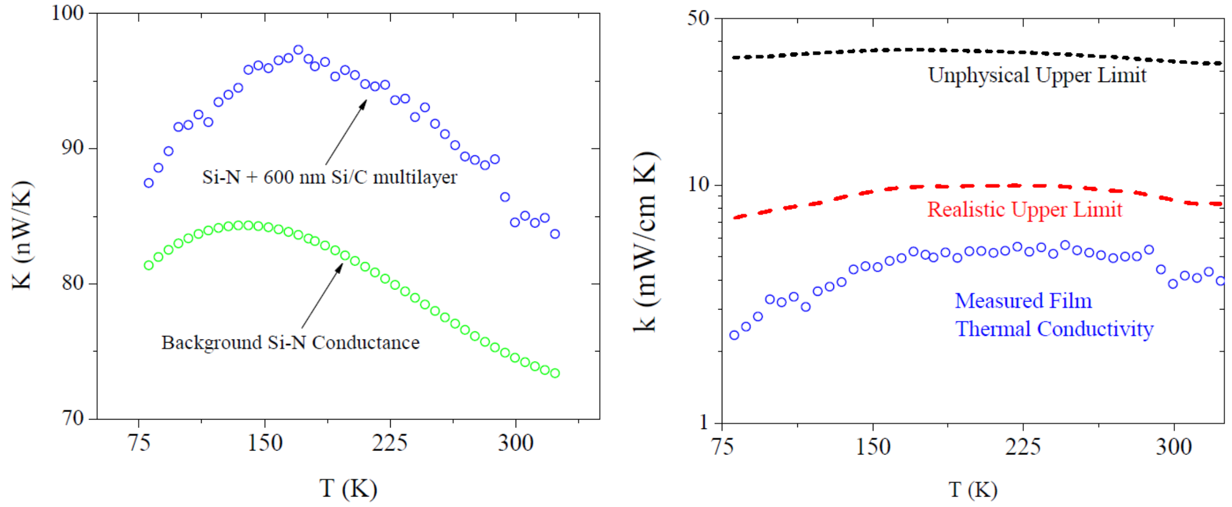


Figure 27 – DU measured thermal conductivity 10nm layer sample as a function of temperature

The total thermal conductivity is the sum of the lattice and electron transport contributions, where the relatively low temperature measurements at DU give the lattice thermal conductivity. The Wiedemann-Franz Law was used to estimate the electron contribution. The figure of merit can also be recast in terms of the Wiedemann-Franz Law to show the importance of reducing the phonon contribution compared to the electron contribution.

Equation 7 – Total thermal conductivity

$$\lambda = \lambda_e + \lambda_p$$

Equation 8 – Electron contribution to thermal conductivity

$$\lambda_e = \frac{L_0 T}{\rho}$$

Equation 9 – Lorenz number

$$L_0 = 2.45 \cdot 10^{-8} \left(\frac{V}{K}\right)^2$$

Equation 10 – Alternative zT estimate using Wiedemann-Franz

$$zT = \frac{\alpha^2}{\rho\lambda} T = \frac{\alpha^2}{\rho(\lambda_e + \lambda_p)} T = \frac{\alpha^2}{\rho\lambda_e\left(1 + \frac{\lambda_p}{\lambda_e}\right)} T = \frac{\alpha^2}{L_0\left(1 + \frac{\lambda_p}{\lambda_e}\right)}$$

The following graph was obtained by using the above equations while measuring both the resistivity and the average temperature and adding them to the λ_p value measured by The University of Denver at 67°C.

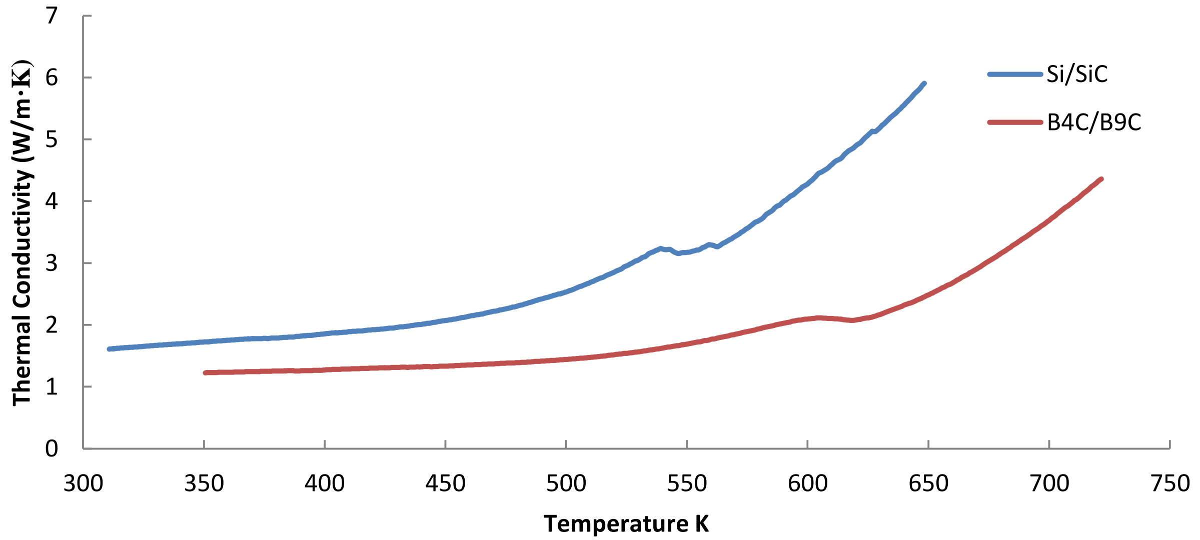


Figure 28 – Thermal conductivity as a function of temperature of 60 layer, 10 nm per layer superlattices deposited at 500°C

NON-DIMENSIONAL FIGURE OF MERIT (ZT)

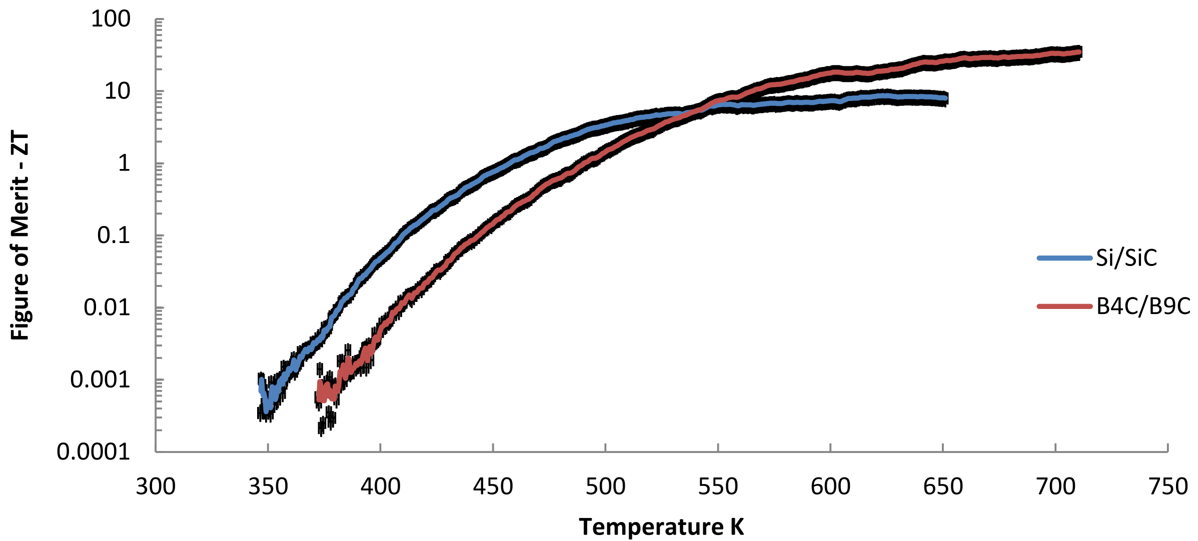


Figure 29 – Measured 10nm layer sample Figure of Merit (zT) as a function of temperature with 25% error bars due to RTD location.

Typical measurements for Si/SiC and B_4C/B_9C lattices deposited at 500°C are listed in the table below. Here, we obtained best zT values of 8.4 and 25.0 at 650 K, respectively. Also listed in the table are the best estimates of Seebeck and resistivity values from (Leavitt, Krommenhoek, Ghamaty, & Elsner, 2010). Figures of merit from the literature data, for comparison, were calculated assuming that the films' thermal conductivity is approximately 1/4th of bulk material as hypothesized by the authors. This bulk thermal conductivity is calculated using a rough combination of the two materials, where quoted bulk properties can vary among sources, and dividing by 4. We note that the thermal conductivity from the measurement at DU indicates the thermal conductivity could be much lower than 1/4th of bulk, increasing the figure of merit in the (Leavitt, Krommenhoek, Ghamaty, & Elsner, 2010) study.

Table 3 – Best measurement results

Material	Temperature	Seebeck	Resistivity	Thermal Conductivity		Figure of Merit
	T	α	ρ	λ_p	λ_e	zT
	°C (K)	mV/K	mΩ-cm	W/(mK)	W/(mK)	-
CSU best measurement:						
Si/SiC	377 (650)	-0.49	0.46	0.8	3.6	8.4
B_4C/B_9C	377 (650)	0.95	0.90	0.8	1.7	25.0
Data from (Leavitt, Krommenhoek, Ghamaty, & Elsner, 2010):						
Si/SiC	25 (298)	-1.20	0.95	25	0.8	1.4
	250 (593)	-1.30	0.55	25	2.3	4.9
	500 (773)	-1.50	0.39	25	4.9	12.6
B_4C/B_9C	25 (298)	1.00	1.10	20	0.7	1.2
	250 (593)	1.05	0.45	20	2.8	5.1
	500 (773)	1.10	0.25	20	7.6	12.4

EFFECTS OF ION ENERGY

The greatest improvement in thermoelectric properties was found to be due to decreasing the ion beam energy striking the sputter targets. The energy of the sputtered atoms from the sputter target is related to the incident ion energy. Reductions in beam ion energy were used in an effort to create sharper material boundaries between the insulating and semi-conducting layers, as reducing the sputtered atom energy reduces the depth to which the atoms implant into the substrate surface. The (average) energy of a sputtered silicon atom, for instance, drops from 14.5 to 9.7 eV in reducing the argon incidence energy from 1200 to 400 eV (calculated using TRIM [Transport of Ions in Matter] from the SRIM [Stopping and Range of Ions in Matter] software package). Dropping from 1200 to 400 eV generated a factor of 2 increase in the Figure of Merit. Sharp edges are believed to create a sharper bending of the bands, which increases the Seebeck coefficient, greatly increasing the Figure of Merit.

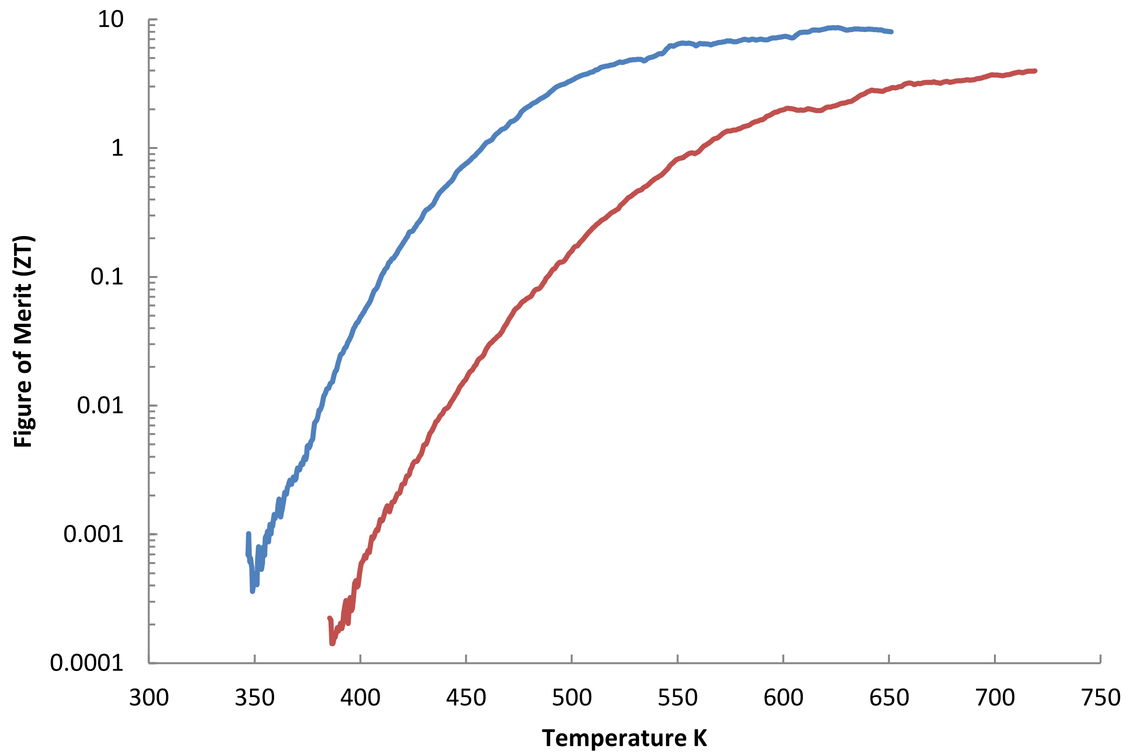


Figure 30 – Comparison of zT for films deposited using two different ion energies

CONCLUSION

An ion beam deposition technique was successfully applied to create n and p-type superlattice films with thermoelectric non-dimensional figures of merit, zT, of 8 and 25, respectively (measured at 650K). The n and p-type superlattices were made from un-doped Si/SiC and B_4C/B_9C. The SiC, B_4C, and B_9C targets were prepared by spreading powders over stainless steel trays that were then placed under the ion beam. The Si target was comprised of 6" polished silicon wafers. Hence the materials of the films were easily obtainable and low cost alternatives to conventional thermoelectric materials. The ion-beam-formed superlattices performed comparatively to superlattices formed using magnetron deposition processes that were reported in the literature. In addition, the rate of superlattice growth with the ion beam system was found to be ~2x faster than magnetron system, which will help reduce the cost of forming TE modules based on these materials.

Thin film processing parameters that were investigated included ion energy, pre-etching condition, layer thickness, layer number, and deposition temperature. The pre-etching of the silicon substrate substantially improved the superlattice resistivity and made the most significant difference in zT compared to the other processing parameters. Decreasing the ion energy increased the zT by a factor of two, and this affect was attributed to sharper boundaries being formed between adjacent layers. Deposition temperature was found to strongly affect film adhesion to the silicon substrate below 300°C, however, deposition temperatures above 400°C resulted in well adhered films. It has been shown that theoretical improvements to zT should continue to increase as the layer thickness decreases. Our tests confirmed that thinner layer superlattices performed better; however, studies were only conducted with layer thickness ranging from 20 nm to 5 nm.

SUGGESTIONS FOR FUTURE WORK

Two main goals are identified for advancing this work. First, to achieve a better understanding of how to maximize zT, a better test apparatus needs to be setup to study materials as they are produced within the vacuum system. In this way, zT as a function of various process parameters can be determined. Second, the manufacturability of modules comprised of many p-n couples needs to be addressed. For thin film superlattice materials to be a viable option for TEG applications, a low cost efficient manufacturing process must be designed.

TEST APPARATUS

Improvements need to be made on the test apparatus. Preferably, a system is preferred that creates repeatable samples, makes connections in situ, and measures thermoelectric properties as a function of temperature in vacuum. The system would include the ability to generate a small, fixed temperature difference across the sample as well as being able to scan the average temperature of the sample over a range from room temperature to 700 K. In addition to allowing higher quality property measurements, an in-vacuum testing station would allow (1) tests to be repeated to verify results and (2) sample aging properties to be assessed.

TEST MATRIX

Using the above described apparatus a test matrix could be created in which the dependence of zT and related thermoelectric properties on deposition temperature, layer thickness, deposition energy, thickness randomness, annealing temperature, etch rate, etc. could be determined while processing.

ION ASSIST

Film delamination at low deposition temperatures was addressed by heating the substrate. This obstacle can also be solved, it is believed, by using an ion assisted deposition system. If an assist ion source was used, then tests could be performed to determine how this improves the adhesion properties of the film as well as how ion assist can reduce internal stresses.

MANUFACTURING AND SUBSTRATE MATERIALS

One of the primary obstacles in creating efficient modules comes from heat loss through the substrate. Any energy passing through the substrate is a complete loss as it performs no useful work. Very thin substrates such as Kapton have been used; however, they are limited in their maximum operating temperatures.

TEG MODULES FABRICATED ON CYLINDRICAL SUBSTRATES

In an effort to achieve high operating temperatures and minimal substrate heat conduction pathway it has been proposed to deposit the super-lattice on a cylindrical substrate on the order of 1µm in diameter. Then, by depositing 1000, 10nm layers, the substrate would make up ~ 0.2% of the cross-sectional area and the module could achieve 99.3% of its predicted maximum efficiency if no substrate were used. A graph of the predicted efficiency as a function of substrate diameter is shown in Figure 31.

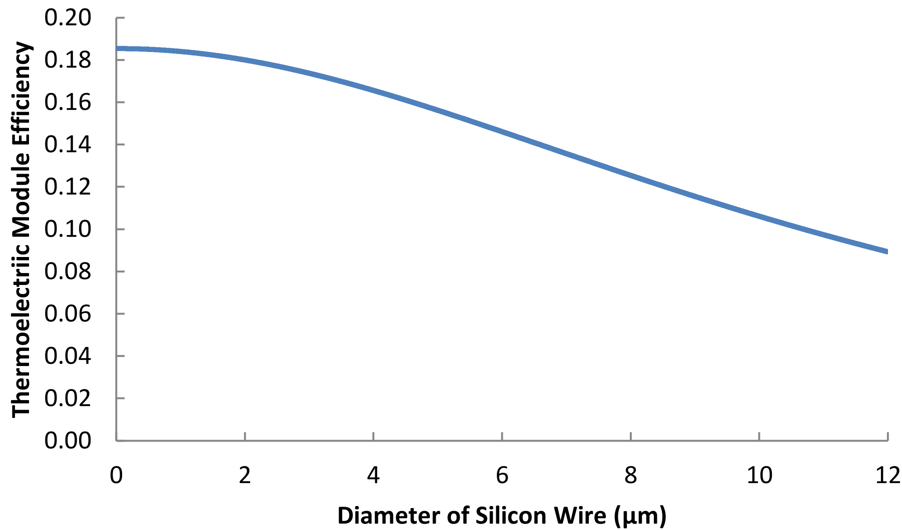


Figure 31 – Theoretical efficiency of thermoelectric vs. diameter of silicon wire substrate. T_h=823K, T_c= 523K, α_p=950 µV/K, α_n=-490 µV/K, ρ_p=0.90 mΩ·cm, ρ_n=0.46 mΩ·cm, κ_p=2.5 W/m·K, κ_n=4.4 W/m·K, 1000 layers, 10 nm layer, Si/SiC, B_4C/B_9C, $\kappa_{substrate}$=150 W/m·K

TEG MODULES FABRICATED ON THIN PLATE SUBSTRATES

Another envisioned substrate geometry is a thin, flat plate made of a material with a low thermal conductivity like ceramic for example. The overall efficiency of a thermoelectric module would depend on the thickness of the substrate legs. The dependence on thickness can be seen in Figure 32. Here it is shown that at a substrate thickness of 0.002" (0.05 mm) we are able to achieve 18.4% efficiency which is 99.3% of the max efficiency were the substrate completely thermally opaque. Ultimately the goal would be to create a multi-module device similar to the one shown in Figure 1. This device would consist of many legs with each sidewall coated with either N or P type materials connected in series to result in the desired operating voltage.

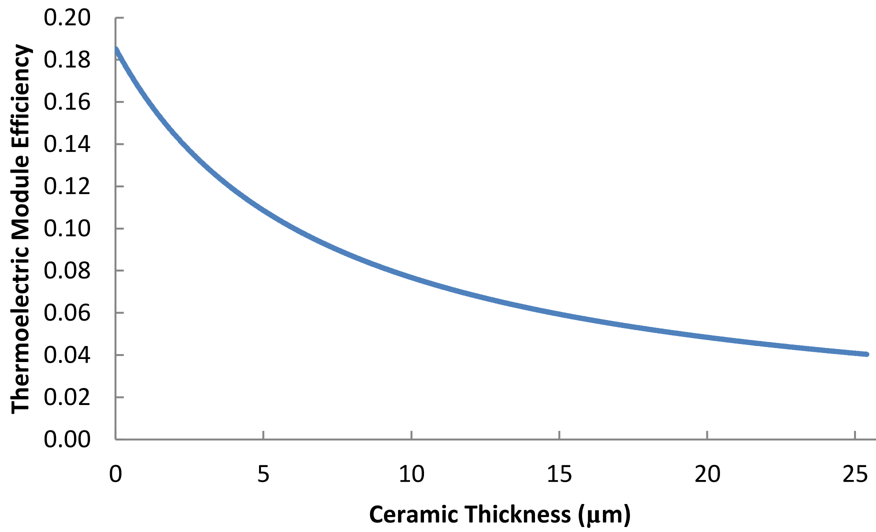


Figure 32 – Theoretical efficiency of thermoelectric vs. thickness of ceramic substrate flat plate geometry, T_h=823K, T_c= 523K, α_p=950 µV/K, α_n=-490 µV/K, ρ_p=0.90 mΩ·cm, ρ_n=0.46 mΩ·cm, κ_p=2.5 W/m·K, κ_n=4.4 W/m·K, 1000 layers, 10 nm layer, Si/SiC, B_4C/B_9C. $\kappa_{substrate}$=2.5 W/m·K

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